SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS FOR HIGH-TEMPERATURE AND RADIATION-RICH ENVIRONMENTS

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SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS FOR HIGH-TEMPERATURE AND RADIATION-RICH ENVIRONMENTS

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Live every act fully, as if it were your last

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SUMMARY

Extreme environments pose unique challenges to all types of electronics. These extreme environments can cover a variety of different conditions, including, but not limited to, low temperatures, high temperatures, radiation, pressure etc. One technology that has shown promising robustness in extreme environments is SiGe HBTs. SiGe HBTs have shown superior performance at low temperatures and are multi-Mrad tolerant to total dose effects. However, a type of extreme environment not often looked at in the context of SiGe HBTs is high temperature and its intersection with radiation. Energy and automotive sectors both have a need for high-temperature electronics while planetary exploration missions to Venus or Jupiter or Saturn require both high-temperature and radiation-tolerant electronics. The objective of this work is to investigate the effects of high temperature (up to 300°C) and radiation on SiGe HBTs, and to provide a framework for building robust, high-temperature capable circuits. In particular, this work aims to explore performance and reliability of SiGe HBTs at elevated temperatures and use this to demonstrate circuit-level operation. Additionally, the intersection of radiation with high temperature is explored to better understand actual space environments. To achieve this objective, DC and AC performance of SiGe HBTs at high temperatures are explored. A safe-operating-area (SOA) map across temperature is generated using a mixed-mode stress methodology to illustrate the reliability concerns. Using this SOA framework, reliable, high-temperature circuits are designed with a calibrated, wide-temperature compact model. Radiation studies were also performed, and their underlying physics is explored with TCAD models. The following is a summary of the contributions from this work:

1. An assessment on the potential of using SiGe-on-SOI HBTs to support emerging applications up to 300°C. This work was presented at the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) 2015, published in BCTM © 2015 [1].

2. An investigation of the total ionizing dose effects on a high-voltage complementary SiGe-on-SOI technology. This work was presented at the IEEE Nuclear and Space Radiation Effects Conference (NSREC) 2016 and published in the IEEE Transactions on Nuclear Science (TNS) © 2017 [2].

3. An investigation of high-temperature (to 300°C) safe-operating-area in a high-voltage complementary SiGe-on-SOI technology. This work was published in the IEEE Transactions on Electron Devices (TED) © 2017 [3].

4. A demonstration of using SiGe-on-SOI HBTs to build 300°C capable analog circuits. This work was presented at the IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) 2018, published in BCICTS © 2018 [4].

5. An investigation on the effects of temperature on the single-event-transient response of a high-voltage complementary SiGe-on-SOI technology. This work was presented at NSREC 2018 and published in IEEE TNS © 2019 [5].

6. A design and demonstration of a high-temperature and high-current gate driver using SiGe-on-SOI HBTs is reported. This work is expected to be submitted to the IEEE Transactions on Electron Device Letters (EDL).

Copyright Statement

CHAPTER 1

MOTIVATION AND BACKGROUND

Silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have found use in a variety of different applications ranging from mixed-mode analog to radio-frequency (RF) and mm-wave circuits [6–8]. The addition of germanium in Si BJTs makes SiGe HBTs competitive with other, more exotic III-V technologies. To date, SiGe HBTs at room temperatures have achieved speeds up to 720 GHz [9]. At cryogenic temperatures, speeds up to 800 GHz have also been reported, thus potentially paving the way for 1 THz SiGe HBTs in the near future [10]. Combined with the low-cost, CMOS integration, and ease of manufacturing, SiGe HBTs are highly desirable for a plethora of circuit applications.

Another appealing aspect of SiGe HBTs is their ability to operate in a variety of different extreme environments (temperature extremes to radiation) [11, 12]. Being able to operate any electronics without additional shielding or temperature control is extremely appealing from a cost and efficiency perspective. However, in order to achieve this, a fundamental understanding of the underlying device is required. This work, in particular, will primarily focus on the operation of SiGe HBTs in high-temperature, radiation-rich environments, and the intersection of both environments. To motivate the need for electronics in these extreme environments, an overview of high-temperature and radiation-rich environments will be discussed. Next, SiGe HBTs will be introduced and their temperature dependence will be presented along with the reliability concerns with increasing temperature. Finally, an overview of radiation effects will be discussed in the context of SiGe HBTs.

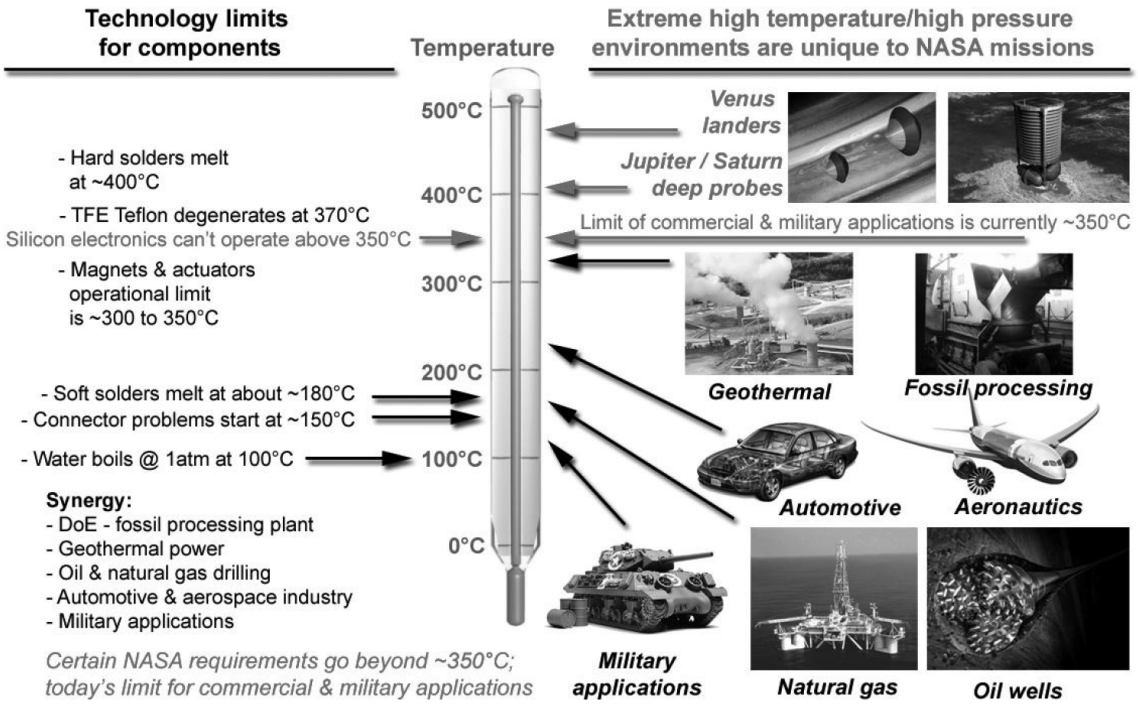


Figure 1.1: The need for high-temperature electronics and the current conventional limits (after [13]).

1.1 Extreme Environments

The field of high-temperature electronics is a rapidly growing market led by various sectors such as aerospace, automotive, energy, and planetary exploration missions [13, 14]. An overview of these different sectors is shown in Fig. 1.1. The need for high-temperature electronics starts as low as 125°C for military applications. With increasing temperature, other sectors come into play such as oil-well digging (150-300°C), automotive (100-300°C), and aerospace (220-500°C).

The energy sector in particular has a clear need for high-temperature electronics due to the increasing demand for energy with the rapid increase in the global economic development. Department of Energy (DoE) projections predict that petroleum will be the major energy source in the next 10-15 years [15]. Petroleum from easily recoverable sources is already rapidly diminishing, and as such, petroleum needs to be recovered from deeper within the Earth. This is achieved with deep wells ($>$ 15,000

feet). Temperatures in these deep wells can reach up to 300°C, and reliable electronics are required. Some examples of the required electronics in these applications are systems needed to control/drive the drill bit along with sensors to monitor external conditions. Geothermal is another energy sector with similar requirements, where temperatures up to 600°C can be encountered [15].

The automotive industry is another major sector driving the need for high-temperature electronics. Modern cars use a mechatronics (mechanical systems + electronics) system design, which requires electronics to operate under-the-hood (150-250°C) or on-engine (200-300°C) [15,16]. Different electronic systems are required in these automotive, high-temperature environments. Power converters (eg: DC-DC converters) and drivers for motor control are needed for the power electronics section, while analog circuits are required for the amplification, signal conditioning and processing applications. While shielding and cooling can be applied to these electronic systems, such an approach adds to the cost and weight of the entire system. Therefore, integrated systems that can inherently handle high temperatures will be critical for optimal design.

Deep-space exploration is another major area where high-temperature electronics are required. A few missions proposed by NASA such as Venus In Situ Explorer (VISE), Venus Mobile Explorer (VME), Saturn Flyby with Shallow Probes (SFSP), and Jupiter Flyby with Deep Entry Probes (JDEP) will require electronics that can tolerate temperatures from 200-480°C [17]. These electronics will range from high-power circuits for power management, driving actuators and motors to high-speed communication and sensing systems.

Additionally, these extraterrestrial missions will require electronics to operate in environments where large amounts of radiation will be present [14, 17]. High-energy particles are routinely encountered in space. These particles typically either originate from the sun or from galactic cosmic rays (GCR) [18]. These high-energy particles

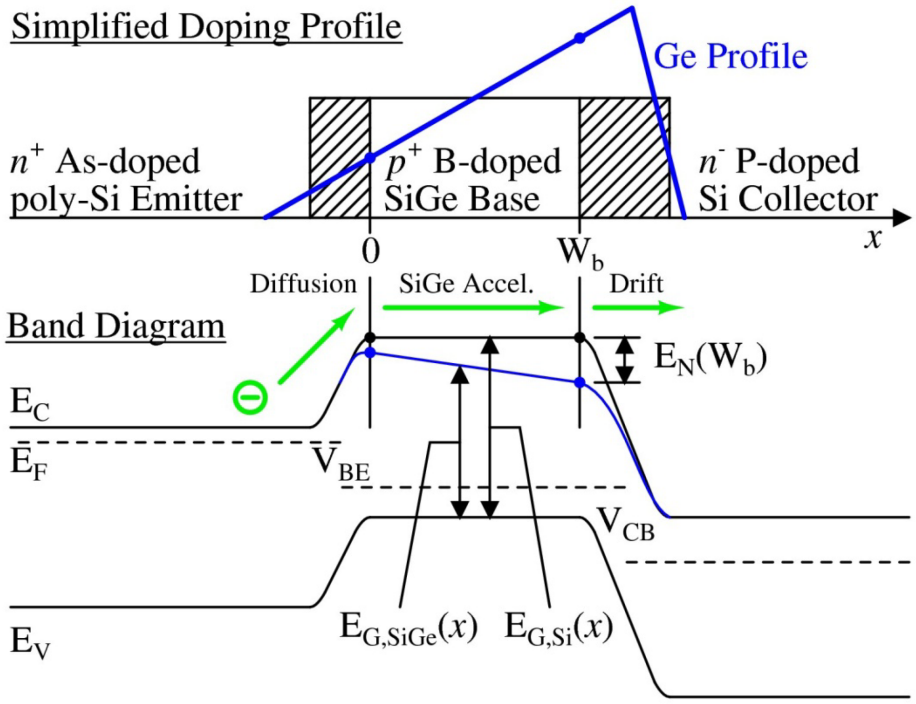


Figure 1.2: A simplified doping profile of a SiGe HBT shown along with the band structure (after [11]).

can be protons, electrons, or heavy ions. Solar events from the sun are of particular interest for electronics in our solar system. For any planet (including Earth) or moon, a magnetosphere traps these high-energy particles and can be a serious threat against planetary exploration. The strength of the magnetosphere has a direct relation to the intensity of the radiation encountered. Therefore, for planets like Jupiter or Saturn, radiation is a significant concern [19, 20]. Similar to temperature, shielding can be used to alleviate the effects of radiation. Typically, aluminum is used to shield sensitive electronics from high-energy particles, but once again, this can significantly increase the cost for space missions since any additional weight has a large monetary cost associated with it. Additionally, significantly high-energy particles (e.g. GCRs) cannot be stopped with shielding.

1.2 Introduction to SiGe HBTs

A SiGe HBT is a close relative to the Si BJT device. In order to understand the differences, it is easier to illustrate it with a simple band diagram as shown in Fig. 1.2. Conceptually, a SiGe NPN (or PNP) device has a similar doping profile as a typical Si NPN (or PNP) device. However, the key difference is the addition of germanium in the base of the device. With clever bandgap engineering, a graded Ge profile can be incorporated into the base of a Si BJT to enhance carrier transport.

As shown in Fig. 1.2, a graded Ge profile has two key effects on the band structure. To understand these effects, it is worth noting the difference in bandgap between silicon (E_g = 1.14 eV) and germanium (E_g = 0.67 eV). The first effect is the reduction in the conduction band barrier (E_C) from the emitter to the base. Even a minute change in the potential barrier has a large effect on the carrier injection as changes in the potential are magnified exponentially [11]. A direct consequence of this reduction in potential barrier is a much higher collector current (I_C) and current gain (β) compared to a Si BJT. This can be observed in Fig. 1.3, where the SiGe HBT is shown to have a significantly larger I_C and β. Additionally, unlike a Si BJT, this decouples the effect of base doping on β. Therefore, the base doping can be tuned independently to decrease base resistance and in turn increase the maximum oscillation frequency (f_{max}), which is not possible in a Si BJT.

The second effect is from the graded Ge leading to a built-in drift field in the base of the SiGe HBT. From an AC perspective, this is highly advantageous as this field reduces the base transit time, which is strongly inversely related to the unity-gain frequency (f_T) of the device. This results in SiGe HBTs achieving f_T of well over 300 GHz rivaling even other III-V devices [9, 21, 22].

A cross-section of a typical SiGe HBT is shown in Fig. 1.4. The intrinsic region of the SiGe HBT consists of a poly-silicon, heavily-doped emitter, a SiGe base, a

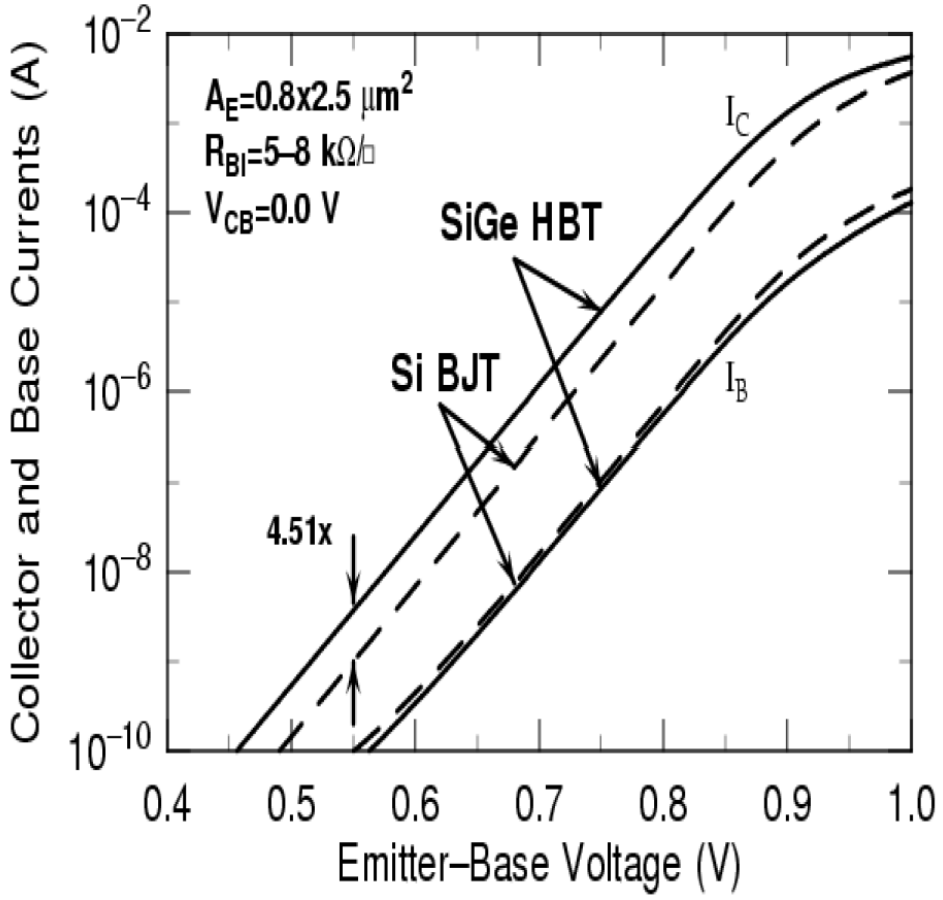


Figure 1.3: Comparison of Gummel curves for "matched" Si BJT and SiGe HBT. Incorporation of Ge is shown to increase I_C by more than 2X (after [11]).

selectively-implanted collector (SIC), and a subcollector. Depending on the technology, the emitter width, base thickness, base doping, and collector doping can all vary drastically. For example, the collector doping can be tailored specifically to achieve different breakdown voltages (BV_{CEO}) or the emitter width can be scaled to reduce parasitics. The extrinsic region of the SiGe HBT consists of different metal contacts and oxides. A shallow-trench isolation (STI) is used to isolate the base contact from the collector contact, while an emitter-base (EB) spacer is used to isolate the emitter contact from the base contact. An additional deep trench (DT) is used to isolate one device from another. It should be noted that there are more advanced SiGe HBTs

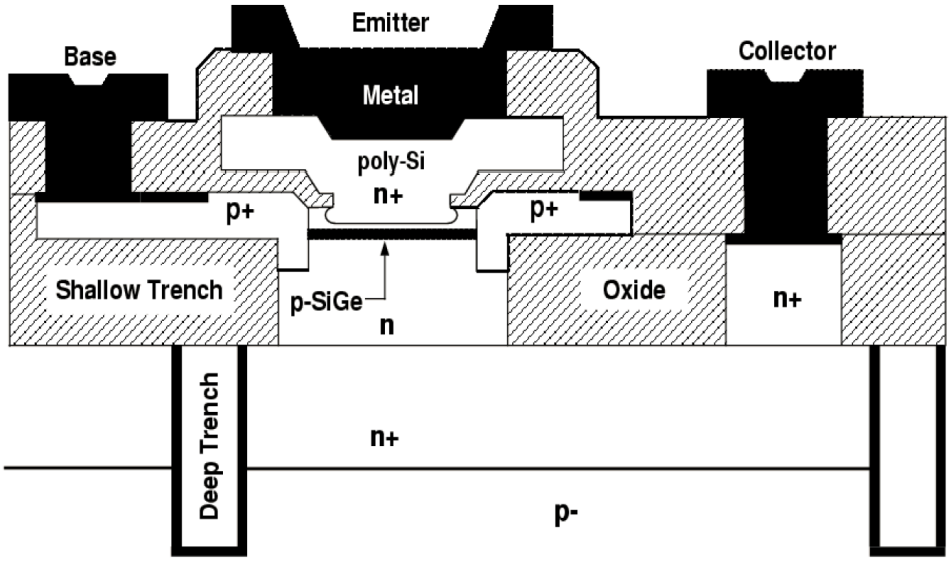


Figure 1.4: Cross-section of a first generation SiGe HBT. (after [11]).

that have completely removed the DT to reduce the overall thermal footprint [23].

SiGe HBT technology is prevalent these days and several different manufacturers offer multiple variants. While CMOS technology can be classified by just the lithography node, the situation is more complex for SiGe HBTs as lithography node alone does not sufficiently describe a device. For SiGe HBTs, it's easier to categorize them by looking at both f_T and $\mathrm{BV_{CEO}}$ since they give an insight into the device speed and the maximum voltage swing they can handle. Fig. 1.5 illustrates some of the different commercial SiGe HBT technologies available today. It becomes very evident that SiGe HBTs come in a variety of different flavors. With careful bandgap engineering and doping profile optimization, it is possible to make SiGe HBTs with an f_T of >400 GHz and a $\mathrm{BV_{CEO}}$ of 1.7 V or a SiGe HBT with an f_T of >5 GHz and a $\mathrm{BV_{CEO}}$ of 48 V. Therefore, this enables SiGe HBTs to tackle a wide variety of different applications. High-speed, low-breakdown devices are highly appealing from a RF/mm-wave applications perspective while low-speed, high-breakdown devices are much more appealing from an analog applications perspective.

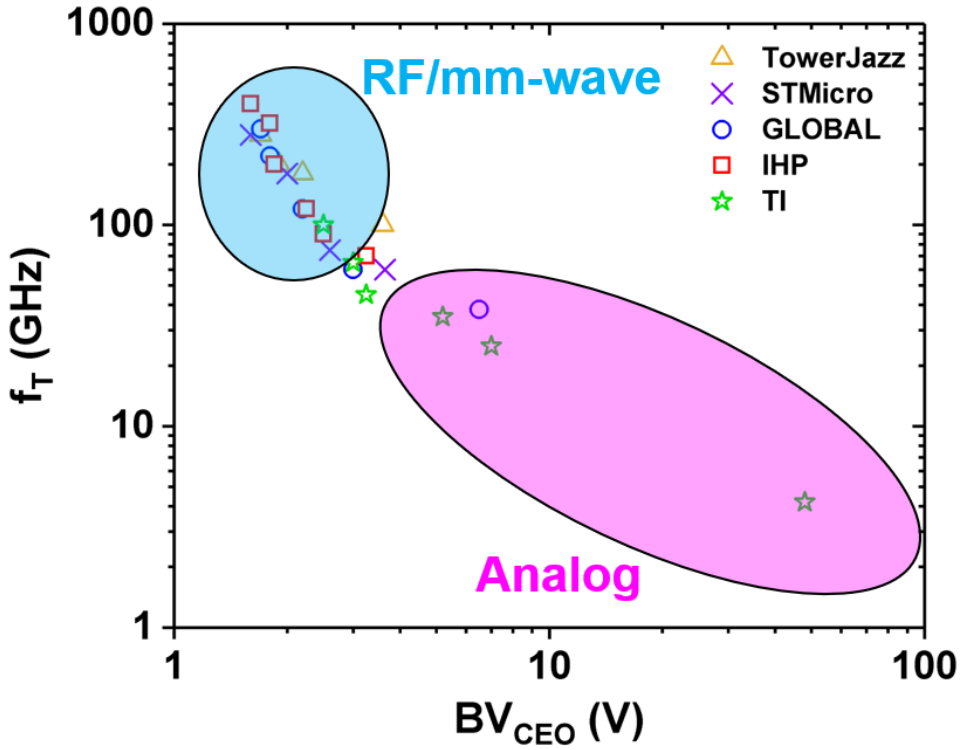


Figure 1.5: f_T as a function of BV_{CEO} for a variety of SiGe HBT technologies from different manufacturers.

A plethora of works in literature has mainly been concerned with the RF/mm-wave optimized devices while not as much light has been shed on the analog optimized devices. This is mainly because there has been a push to achieve III-V semiconductor speeds with silicon (like the DOTFIVE and DOTSEVEN project [9, 24, 25]), which has naturally resulted in a larger focus on those devices. However, this does not mean the analog optimized devices are any less important as SiGe HBTs can provide as much advantage in this particular niche as it can in the RF/mm-wave realm. A part of this work will be to expand on these analog optimized devices and demonstrate some of the subtle difference in physics they have compared to the RF/mm-wave optimized devices.

1.3 Temperature Dependence of the Operation of SiGe HBTs

To understand the temperature dependence of the operation of SiGe HBTs, the relevant metrics of interest need to be identified. For any bipolar technology, there are essentially four key metrics that define the total device performance: β, Early voltage (V_A), f_T, and f_{max}. These metrics have a unique temperature dependence relative to Si BJTs due to the incorporation of germanium in the base of the HBT. Therefore, it is more convenient to quantify these metrics relative to Si BJTs.

The β of SiGe HBTs can be defined as [11] :

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \left\{ \frac{\widetilde{\gamma}\widetilde{\eta}\Delta E_{g,Ge}(grade)/kT \; e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(0)/kT}} \right\} \tag{1.1}$$

where $\widetilde{\gamma}$ is an effective density-of-states ratio between SiGe HBTs and Si BJTs, $\widetilde{\eta}$ is the minority carrier diffusivity ratio between SiGe HBTs and Si BJTs, $\Delta E_{g,Ge}(grade)$ is the germanium induced change in bandgap from the base-emitter interface to the collector-base interface, $\Delta E_{g,Ge}(0)$ is the germanium induced bandgap change at the base-emitter interface, k is the Boltzmann constant, and T is temperature [11]. From (1.1), it can be seen that the dominant temperature term is the exponential $1/kT$ dependence. Therefore, with increasing temperature, β will decrease.

A similar relationship can be established for V_A as [11]

$$\frac{V_{A,SiGe}}{V_{A,Si}} = e^{\Delta E_{g,Ge}(grade)/kT} \left\{ \frac{1 - e^{\Delta E_{g,Ge}(0)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right\} \tag{1.2}$$

Like β, the dominant temperature term is the exponential $1/kT$ dependence. Since V_A is directly proportional to this term, it also has a negative temperature coefficient. Lastly, f_T and f_{max} can be described by:

$$f_T = \frac{1}{2\pi\tau_{ec}} \tag{1.3}$$

$$\tau_{ec} = \tau_e + \tau_b \tag{1.4}$$

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\widetilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[1 - e^{\Delta E_{g,Ge}(0)/kT} \right] \right\} \tag{1.5}$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}} \tag{1.6}$$

where τ_{ec} is the total transit time from the emitter to the collector, τ_e is the emitter transit time, τ_b is the base transit time, C_{bc} is the base-collector capacitance, and r_b is the base resistance [11]. To the first order, maximum value or peak f_T is dominated by τ_b. The temperature dependence of τ_b can be understood by looking at (1.5). There is approximately a direct linear relationship between temperature and τ_b, where τ_b increases with temperature. Therefore, f_T will decrease with increasing temperature, and since f_{max} is directly proportional to f_T, f_{max} has the same temperature dependence.

Since all the relevant metrics clearly show a negative temperature coefficient, it might be tempting to say that SiGe HBTs are not suitable for high-temperature operation. However, the operation of SiGe HBTs up to 300°C has been investigated before, and it was shown that SiGe HBTs, even with performance degradations, achieved acceptable performance for certain applications [1,26]. The work in [1] studied the high-temperature performance of a 150/180 GHz f_T/f_{max} SiGe HBT, where a current gain > 100 and a $f_{max} > 100$ GHz was achieved even at 300°C. While the same room-temperature performance cannot be achieved at elevated temperatures, it is abundantly clear that SiGe HBTs can be used for high-temperature circuits without severe compromises.

Another key device aspect to be considered at elevated temperatures is the reverse-bias p-n junction leakage current (I_0). This leakage current is proportional to temperature through the following relation:

$$I_0 \propto n_i^2 \propto T^3 e^{E_{g0}/kT} \tag{1.7}$$

where n_i is the intrinsic carrier concentration and E_{g0} is the bandgap at $T = 0$ K [16]. The relation shows that the leakage current has strong dependence on the intrinsic carrier concentration, which in turn has approximately a cubic dependence on temperature. To first order, this leakage current doubles for every 10°C increase. This can be a major issue for any silicon-based electronics for high-temperature operation since it increases the overall power consumption. There are some means to overcome this obstacle. One is to use wide-bandgap semiconductors such as gallium-nitride (GaN) or silicon-carbide (SiC), which can be operated to temperatures as high as 600°C due to a larger bandgap resulting in lower leakage current [27–30]. However, using these III-V semiconductors can be more costly than their Si counterparts, and they are not as easy to integrate with CMOS. Another way is to use silicon-on-insulator (SOI) technology. SOI technologies utilize an oxide that isolates the subcollector from the underlying substrate [31,32]. This insulation significantly reduces the leakage current, since the majority of the reverse-bias leakage current at elevated temperatures is due to the collector-substrate junction.

In summary, SiGe HBTs, while performing worse at elevated temperatures, can be operated with acceptable performance even at temperatures as high as 300°C. Additionally, the leakage current associated with increasing temperature can be greatly suppressed by using SOI technologies. Thus, SiGe HBTs can potentially be used for applications requiring operation at high ambient temperatures.

1.4 Temperature Dependence of the Reliability Degradation Mechanisms

Any device technology has a safe-operating-area (SOA) that clearly highlights the safe voltage and current conditions under which the device can be operated without reliability concerns. To map out the SOA trends across temperature for a device technology, key reliability failure regions and mechanisms need to be identified. A sample SOA map is illustrated in Fig. 1.6. There are two main boundaries that play a key role in the limits of viable operation; namely $J_{C,Kirk}$ and BV_{CEO}. $J_{C,Kirk}$ establishes the collector current density at which the Kirk effect dominates device behavior and marks the transition into the high injection regime. BV_{CEO}, on the other hand, establishes the voltage boundary at which collector-emitter breakdown is observed, and sets a conservative upper limit for maximum reliable voltage swing allowed. The other two important regions include the electromigration threshold and the maximum power output. The maximum power output region is more of a hard limit arising from device parasitics and power dissipation of the material itself and thus will not be investigated here.

From a pure electrical perspective, there are two main degradation mechanisms that can play a vital role in SiGe HBT reliability: avalanche breakdown and Auger damage. Both of these degradation mechanisms and their respective operative regions are illustrated in Fig. 1.6. Both avalanche breakdown and Auger damage are initiated by hot carriers (or high-energy carriers) traversing the device and reaching sensitive oxides to create interface traps, thereby leading to parasitic leakage current [33]. Avalanche breakdown is triggered by the large electric field in the reverse-biased collector-base (CB) junction that leads to the creation of hot carriers through the avalanche multiplication process. This is visually shown in Fig. 1.7. Hot carriers generated by this field have a position and temperature dependence probability of reaching either the EB spacer or STI oxide. Additionally, there is also a probability

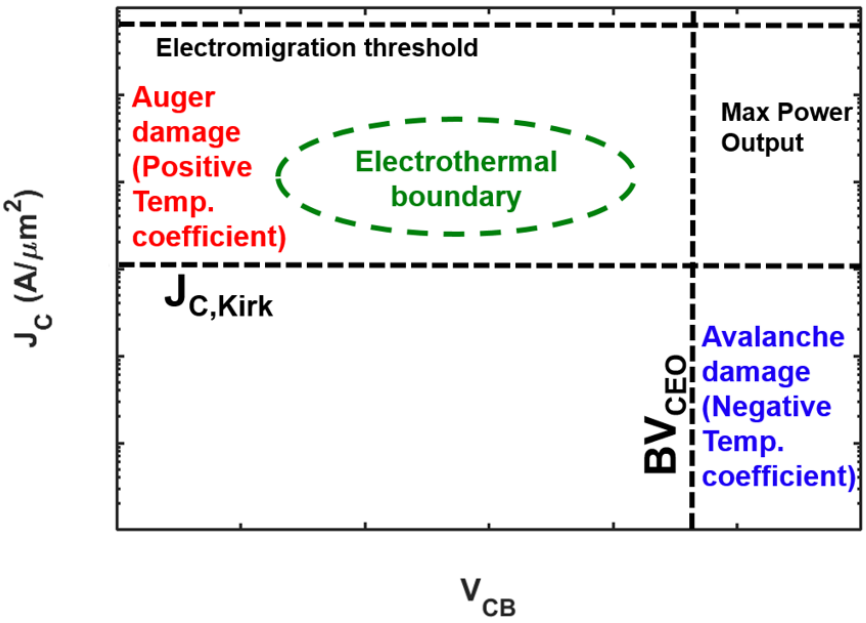


Figure 1.6: General SOA map highlighting the J_C-V_{CB} plane for SiGe HBTs along with the different reliability degradation regions and operative damage mechanisms.

associated with a hot carrier having enough energy at the point of collision. This is largely determined by the mean free path length, which has a strong temperature dependence. Avalanche breakdown is directly related to the M-1 (avalanche multiplication factor) metric, which is easily measured and can be used to understand the underlying temperature dependence.

Another key degradation mechanism is Auger damage. Auger recombination is a similar mechanism as avalanche breakdown, in that it produces hot carriers but in this case it is driven by high current density rather than large electric fields. Auger recombination requires three carriers to occur, where an electron and hole recombine and excite the third electron to a higher energy state. However, a single recombination event alone will not produce a hot carrier with enough energy to cause damage at the oxide interfaces. Therefore, this mechanism is only relevant at sufficiently

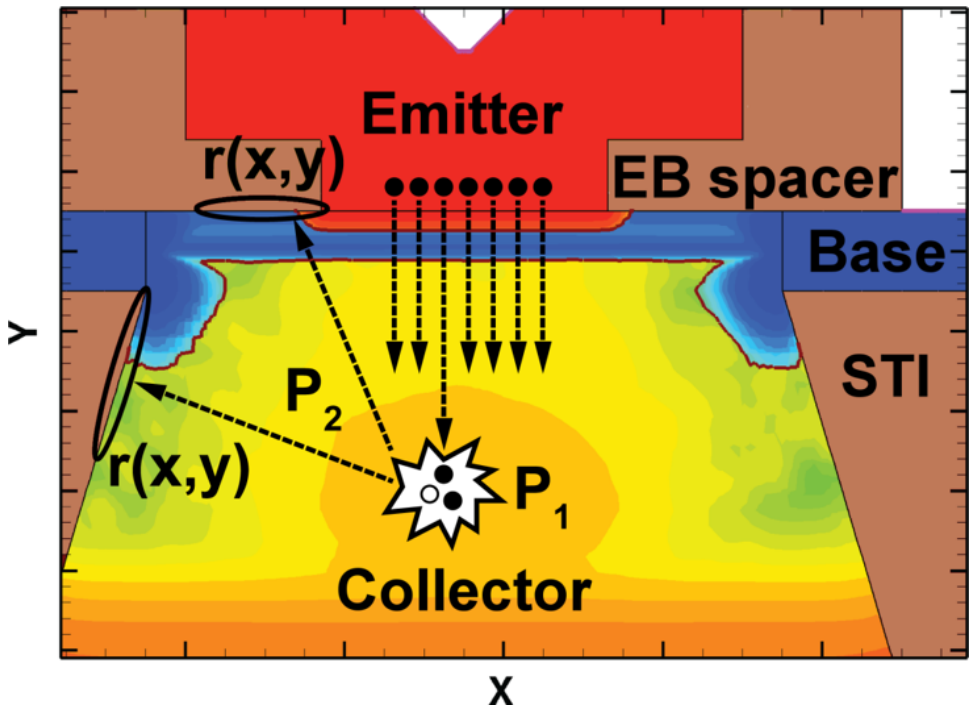


Figure 1.7: Device cross-section illustrating the physical location of hot carrier generation and the sensitive oxides (after [33]).

high current density, such that there are enough recombination events for a carrier to gain sufficient energy (2.3 eV) to cause damage to the oxide interfaces [34]. Unlike avalanche breakdown, the generation of hot carriers for the Auger recombination process does not occur at the CB junction. Since Auger recombination requires large current densities, the peak Auger recombination rate is expected to be closer to the EB junction and therefore making the EB spacer more susceptible to damage. The temperature dependence of Auger damage has been highlighted in [35]. Essentially, the Auger recombination rate and the hot-carrier energy distribution function (EDF) play a key role in the temperature dependent behavior of Auger damage. As both the recombination rate and EDF increase with increasing temperature, from a high-temperature perspective, Auger damage is likely to be a limiting factor at high currents, since it will act to effectively reduce the maximum allowable current.

While Auger damage and avalanche breakdown cover the key degradation mechanisms for SiGe HBTs, electrothermal constraints are also significant in defining the resultant SOA. Electrothermal constraints mainly arise from device self-heating due to large power dissipation [36, 37]. The extent of device self-heating varies between different device technologies due to differences in device structure and the oxide interface area and location. It can also be a bigger problem for SiGe HBTs due to the higher current density compared to Si BJTs. A major factor that can severely influence device self-heating is the presence or absence of buried oxides in SOI technologies. An underlying oxide beneath the subcollector can restrict heat flow due to its reduced thermal conductivity, leading to more severe self-heating than for bulk devices. Previous work has investigated the electrothermal behavior of SiGe HBTs across temperature [1]; however, the electrothermal behavior was only examined for a single collector current density and not across the whole SOA region.

Outside of device-level reliability, electromigration is a significant concern when operating any electronics at high temperatures. Electromigration is the movement of metal atoms in metal lines that can lead to an electrical open or short [16, 38]. The mean time to failure (MTTF) of any metal line can be described using Black's equation

$$MTTF = AJ^{-n}e^{E_a/kT} \tag{1.8}$$

where A and n are constants, J is the current density, k is the Boltzmann constant, T is temperature, and E_a is the activation energy [16]. With increasing temperature, there is a clear decrease in MTTF. Thus, electromigration is a big concern for circuits operating at elevated temperatures ($> 200°$C). In order to mitigate electromigration related issues, large metal widths for current handling are required.

The different reliability degradation mechanisms and their underlying physical temperature dependences are discussed in the context of SiGe HBTs. However, no

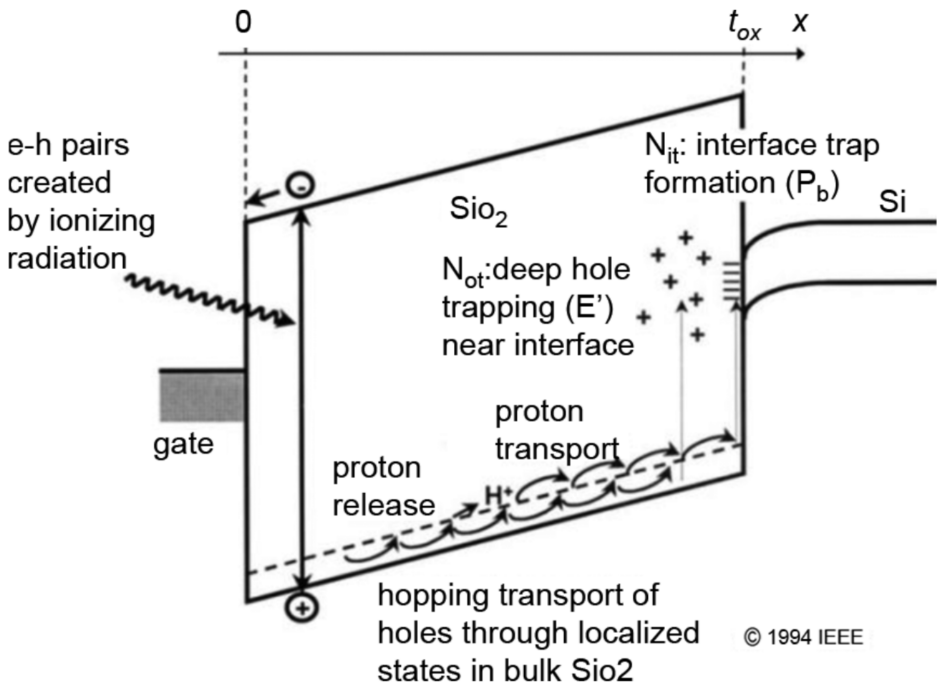


Figure 1.8: Generation of charge and interface traps in a MOS structure after TID (after [40, 41]).

measured reliability data for SiGe HBTs exists up to 300°C. In order to build reliable circuits and systems aimed at high-temperature operation, a comprehensive mapping of the temperature trends of the SOA is required.

1.5 Radiation Effects in SiGe HBTs

As highlighted previously, for deep-space missions, electronic systems can encounter both high temperatures and large amounts of radiation. The effects arising from this radiation can be classified as displacement damage (DDD), total ionizing dose (TID), single-event effects (SEE). Displacement damage was found to be insignificant in SiGe HBTs because of the heavy doping in the base and emitter, and therefore will not be explored further in this work [39].

TID is an effect arising from high-energy particles transferring energy to sensitive oxides in devices [41]. The unit of measurement for TID is rad, which stands for

radiation absorbed dose. Since rad is material dependent, it is important to clarify which material is being referred to when citing total dose accumulated. For SiGe HBTs, this is usually referred to in the context of SiO_2. The exact TID mechanism is shown in Fig. 1.8. High-energy particles deposit energy to an oxide, which results in the generation of electron-hole pairs (EHPs). Electrons diffuse out of the oxide quickly, while holes tend to stay in the oxides due to their lower mobility. This can result in both the accumulation of positive charge within the oxides and the formation of interface traps along the oxide-silicon interface. The interface trap formation occurs due to trapped holes eventually reaching the oxide-silicon interface and displacing a hydrogen bonded with oxygen [42, 43].

In the context of SiGe HBTs, the accumulation of traps can lead to an increase in the base leakage current at low base-emitter voltage (V_{BE}). Consequently, an increase in base current leads to a reduction in β, and thus degrades the device performance. Positive charge accumulation can also negatively affect device performance since it can effectively change the emitter area and consequentially, the I-V characteristics [44]. The effects of TID on SiGe HBTs have been studied across several SiGe HBT generations using both X-ray and gamma sources [12,45]. All the studies have clearly shown that SiGe HBTs are tolerant to multi-Mrad doses, which are typically not encountered in near-Earth missions but are relevant in more harsh radiation environments such as Jupiter. From a temperature perspective, the effects of cryogenic temperatures on the TID response of SiGe HBTs used in a bandgap reference circuit (BGR) was briefly studied in [46]. The results indicated that the TID-induced damage was minimal even at cryogenic temperatures.

The second key radiation effect is SEE. SEE is a result of high-energy particles such as electrons, protons, and heavy ions traversing through the active volumes in a semiconductor device, which can be either destructive or non-destructive [12, 42, 48, 49]. Some destructive SEE is single-event burnout (SEB), single-event latch-up

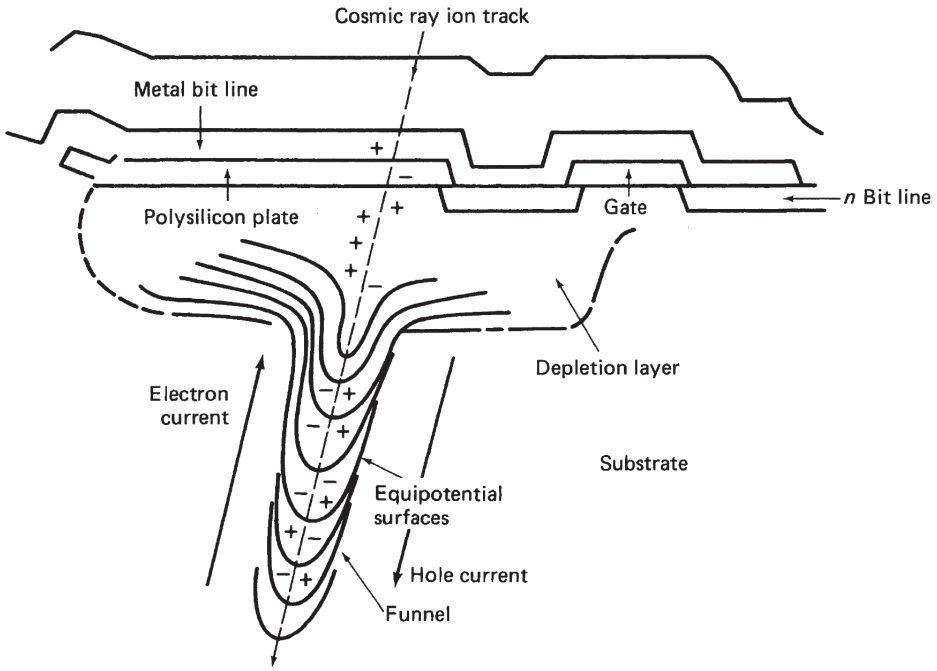


Figure 1.9: Ion-track in a DRAM cell highlighting the formation of a "funnel" that collapses the depletion layer within the device (after [47]).

(SEL), and single-event gate rupture (SEGR). SEB typically occurs in power devices while SEL and SEGR are more relevant in CMOS technology. Non-destructive SEE like single-event upset (SEU), single-event transient (SET), and multiple-bit upset (MBU). For CMOS, SEU and MBU can cause bit-flips, which can potentially corrupt data.

SETs, however, are very relevant in SiGe HBTs. As a high-energy particle traverses through the sensitive volume, a track of electron-hole pairs (EHP) is generated as shown in Fig. 1.9. This momentarily causes all the junction electric fields to collapse and is known as the "ion-shunt effect" [50]. Eventually, the junctions begin to re-establish themselves and the excess carriers are swept out by diffusion through the device terminals. This results in transient pulses at the device terminals. These transient pulses can then propagate through a larger circuit/system and potentially disrupt performance or even corrupt data [51–53]. Unlike TID tolerance, SiGe HBTs

are highly susceptible to SETs [54–56]. In fact, due to their vertical structure, it can even be said that they are more susceptible to SETs than FETs.

In the context of temperature, some prior work has been performed on the effects of temperature on SEE for diodes and CMOS devices [57–61]. The work in [57] examined the temperature dependence of transients for $p^+/n/n^+$ epilayer diodes, and found that the transient peak amplitude decreases with increasing temperature, while the collected charge is fairly temperature independent. Simulation work has been performed on the cryogenic single-event transient (SET) response of SiGe HBTs in [62], and the transient peak amplitude was found to increase with decreasing temperature. While SEE in SiGe HBTs has been reported in literature before, there is a gap in knowledge of the effect elevated temperatures can play a role in SEEs. Bridging this gap can enable the use of SiGe HBTs for potential deep-space missions, where high-temperature and radiation effects will be encountered.

1.6 Thesis Layout

The key objective of this work is to investigate the effects of high-temperature and radiation on SiGe HBTs and provide a framework for building robust, high-temperature capable circuits. This thesis is structured into 8 chapters: 1) Motivation and Background, 2) SiGe-on-SOI HBT Operation at High Temperature, 3) Reliability of SiGe HBTs at High Temperatures, 4) Building High-Temperature Capable Analog Circuit Building Blocks Using SiGe HBTs, 5) High-Temperature Gate Driver, 6) Total Ionizing Dose Effects in a High-Voltage SiGe HBT Technology, 7) Temperature Dependence of Single-Event Effects, 8) Conclusions and Future Work. Chapter 1 is meant to give a background on extreme environments and how SiGe HBTs play a role in it. Chapters 2-5 will primarily cover high-temperature related work. Chapter 2 shows the DC and AC performance of SiGe HBTs up to 300°C. Chapter 3 covers the temperature scaling of the reliability degradation mechanisms in SiGe HBTs. Chapter 4 covers the design and operation of high-temperature capable analog circuit building blocks. Chapter 5 shows the operation of a more sophisticated high-temperature capable gate driver circuit. Chapters 6-7 will primarily cover radiation related work. Chapter 6 investigates the TID effects in a high-voltage SiGe technology. Chapter 7 covers the temperature dependence of single-event effects. Chapter 8 concludes this thesis with the main contributions and potential future work that is possible based on this work.

CHAPTER 2

SIGE-ON-SOI HBT OPERATION AT HIGH TEMPERATURE

Several studies have reported on the operation of high-speed SiGe HBTs in extreme environments, particularly at cryogenic temperatures and in radiation-rich environments [63–65]. Due to the nature of the exponential dependence on temperature, SiGe HBTs enjoy an appreciable increase in most DC and AC key figures-of-merit (FoM) at reduced temperatures [64]. Record performance of 0.8 THz f_{max} was demonstrated at 4.3 K for a high-speed SiGe HBT, thus lending credence to the capabilities of SiGe HBTs operating at extremely low temperatures [10].

However, the operation of SiGe HBTs on the higher end of the temperature spectrum has not been explored as much as cryogenic temperatures. Recent work for a bulk SiGe HBT with an f_T of 120 GHz were published in [26], while SiGe HBTs on thin-film SOI with a peak f_T of 35 GHz were reported in [66]. The work in [26] illustrated favorable DC, AC, and low noise performance, even at elevated temperatures, but the use of bulk devices resulted in high off-state leakage current. A CMOS compatible thin-film SOI was used in [66], which was more suitable for high-temperature operation, but at the cost of significantly lower AC performance.

High-temperature electronics has emerged as a field of recent interest, with applications in automotive electronics, aviation electronics, oil well digging, and even radar systems [26, 67]. In particular, telemetry applications (e.g., deep oil well digging and space electronics) require high-speed devices. For bulk devices, wide-bandgap semiconductors such as SiC or GaN have been looked at for high-temperature operation due to lower intrinsic concentration even at elevated temperatures (leading to lower

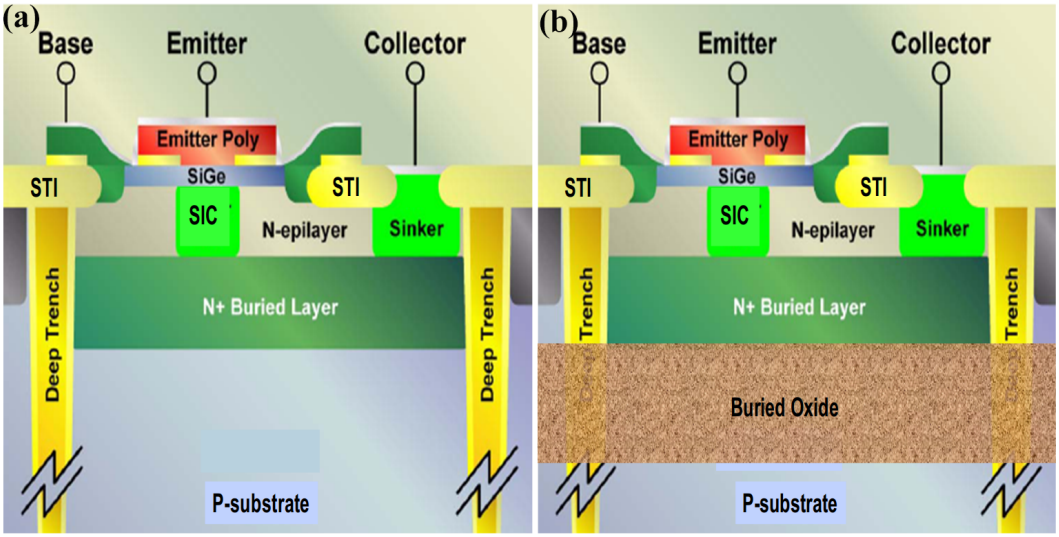


Figure 2.1: Cross-section of (a) bulk, (b) SOI SiGe HBT.

leakage current) [68]. As lower temperature favors the SiGe HBT performance, it also leads to degraded performance with increasing temperature. As such, high-speed SiGe HBTs have not been considered applicable in the realm of high-temperature electronics. However, with modern SiGe HBTs routinely reaching >120 GHz performance at room temperature, it is likely that device performance will remain high enough with temperature. The use of SOI can alleviate the leakage currents at high temperatures while offering other benefits such as isolation, reduced parasitics, and lower sensitivity to single event upsets (SEU) [66]. SiGe HBTs on thick-film SOI can provide several benefits at temperatures up to 300°C, especially from a speed perspective compared to bulk BJT silicon devices, and are becoming increasingly common.

Prior studies show that the use of SOI, however, tends to increase the thermal resistance (R_{th}) due to the poor thermal conductivity of SiO_2 that can lead to strong self-heating and electrothermal runaway at high DC power [69]. High-performance SiGe HBTs are already aggressively scaled and this contributes to strong self-heating resulting from the larger current densities and electric fields [36]. In this chapter, for the first time, the high-temperature operation of 120/180 GHz f_T/f_{max} SiGe HBTs

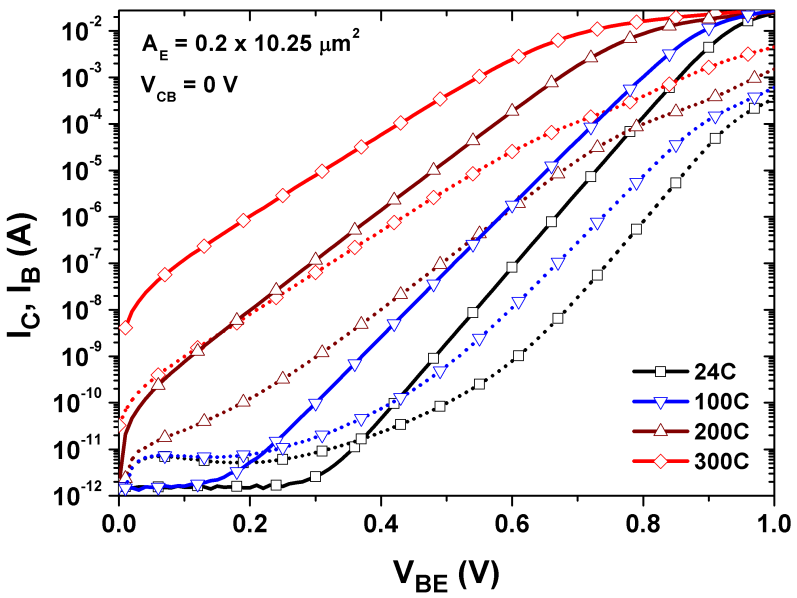


Figure 2.2: Forward-mode Gummel (SOI) for 24°C, 100°C, 200°C, and 300°C. Solid lines are I_C while dotted lines are I_B.

on SOI technology is explored, and the data show that the devices can be reliably operated up to 300°C without severe electrical or thermal degradation.

2.1 Technology and Measurement Details

The devices used in this study are a 0.2 x 10.25 μm^2 SiGe *npn* on SOI (and bulk), with a peak f_T/f_{max} of 120/180 GHz. A simplified cross-section for the bulk and SOI device is shown in Fig. 2.1 [70]. The devices contain both STI and DT isolation and were not optimized for high-temperature operation. Aside from the substrate differences, the SOI and bulk devices are completely identical.

Both DC and AC measurements were made on-wafer on a hot chuck capable of operating from 24°C (room temperature) to 300°C. An Agilent 4155C parameter analyzer was used to make all DC measurements, while an Agilent E8316C network analyzer was used to make S-parameter AC measurements.

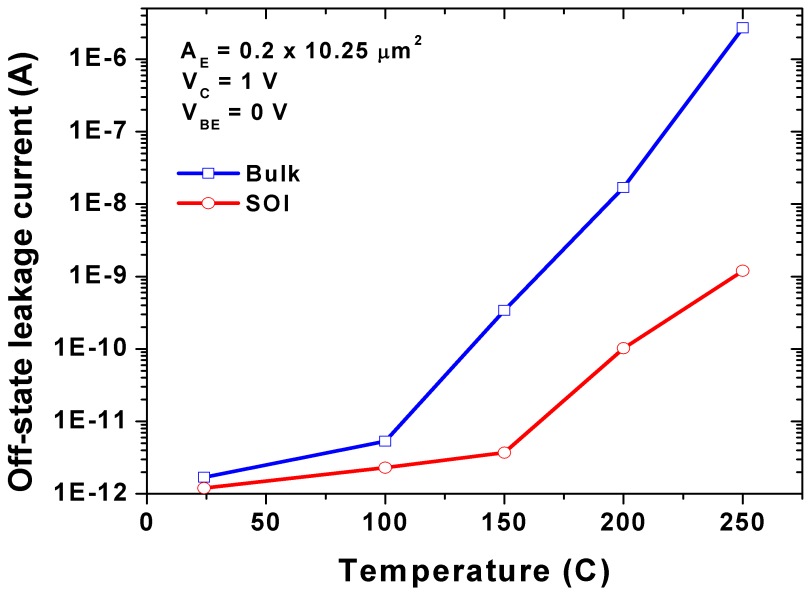


Figure 2.3: Off-state leakage current (I_C) as a function of temperature for both bulk and SOI devices.

2.2 Results and Discussion

2.2.1 DC Characteristics

The DC characteristics at high temperature were measured using the forward-mode Gummel with $V_{CB} = 0$ V, from 24°C to 300°C, as illustrated in Fig. 2.2. The Gummel characteristics remain nearly ideal over a wide temperature range, indicating normal operation. No deleterious series resistance effects were seen at high injection, as shown by the steady increase in collector current up to 300°C. Due to the SOI substrate, off-state leakage current is suppressed at high temperatures relative to the bulk device. This is illustrated in Fig. 2.3 where a three orders of magnitude difference between the off-state leakage current at 250°C results from the use of SOI. This low off-state current is advantageous for many analog applications.

Forward-mode current gain (β_F) data from 24°C to 300°C are shown in Fig. 2.4. The peak β_F decreases with temperature, which is consistent with theory [11]. Although the data show approximately a 40% decrease in peak β_F at 300°C relative to

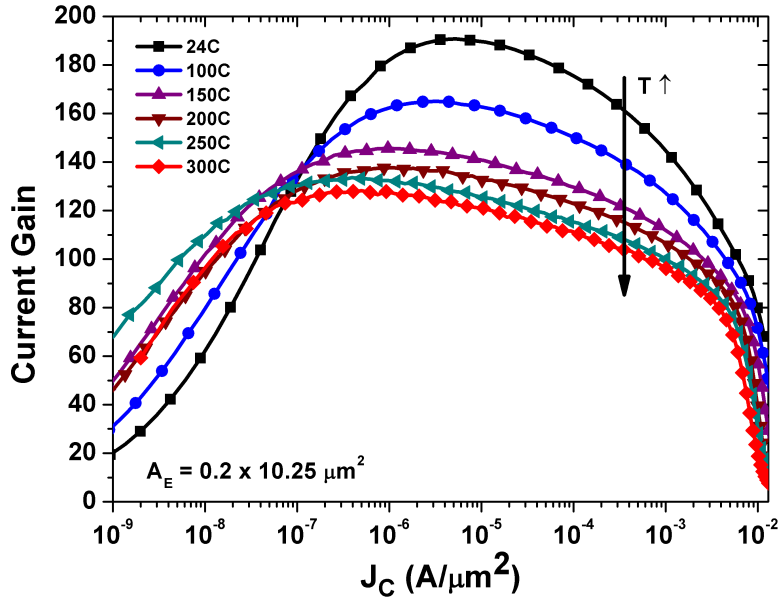


Figure 2.4: Forward-mode current gain (β_F) from 24°C to 300°C for SOI.

24°C, the device still yields a gain of over 100, demonstrating that these devices have adequate 300°C gain for most analog applications. An unexpected trend is observed at low injection, where the β_F increases with temperature up to 250°C. This disparity is attributed to the excess base current leakage found at 24°C in Fig. 2.2. Until 250°C, the collector current increases faster than the base current leading to an increasing β_F at low injection.

One area where SiGe HBTs have an advantage with increasing temperature is in collector-emitter breakdown voltage (BV_{CEO}). BV_{CEO} values were extracted using the technique in [11]. Fig. 2.5(a) shows that there is close to 25% increase in BV_{CEO} from 24°C to 300°C. This is another positive factor for circuits operating at high temperature. Since BV_{CEO} is directly related to both β_F and the impact ionization rate (M-1), the behavior of M-1 over temperature was also measured and analyzed. M-1 as a function of V_{CB} over temperature is plotted in Fig. 2.5(b). With increasing temperature, the impact ionization rate decreases, as previously reported in [26, 66]. This is attributed to higher phonon scattering at elevated temperatures

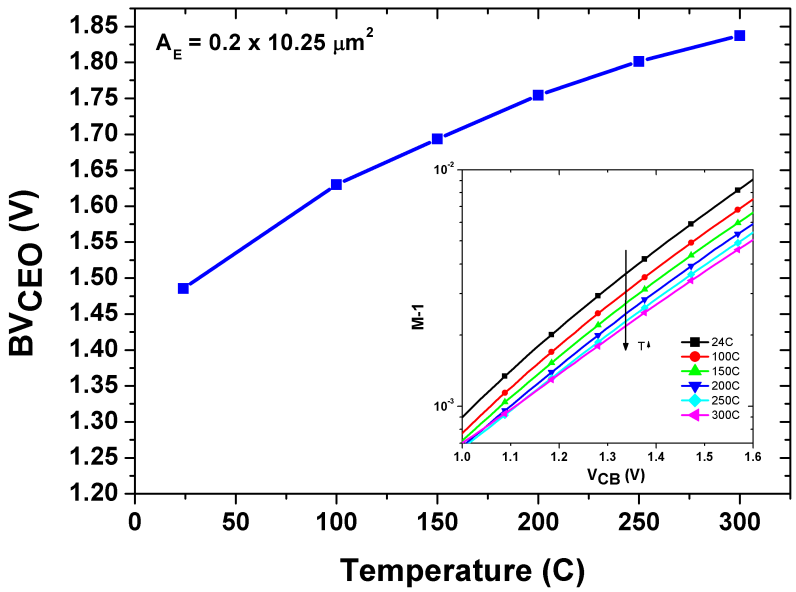


Figure 2.5: (a) BV_{CEO} as a function of temperature for SOI, (b) M-1 as a function of V_{CB} from 24°C to 300°C for SOI.

that decreases the probability of an electron causing impact ionization, which is highly advantageous from a reliability perspective. Since both M-1 and β_F are decreasing with temperature, it supports the observed BV_{CEO} trend over temperature.

2.2.2 Thermal Effects

Prior work have been reported on the positive temperature coefficient of R_{th} in SiGe HBTs [26, 66]. Thus, self-heating effects are expected to worsen with increasing temperature. R_{th} was extracted using similar technique as described in [71] and is plotted across temperature in Fig. 2.6 for both bulk and SOI devices. R_{th} increases for both devices, however, the bulk device shows a higher rate of increase relative to SOI. We note that the device measured is a single emitter geometry and the thermal resistance can be significantly reduced by using multi-fingered devices instead [26]. The self-heating effects leading to thermal runaway at room temperature for these devices were previously reported in [36].

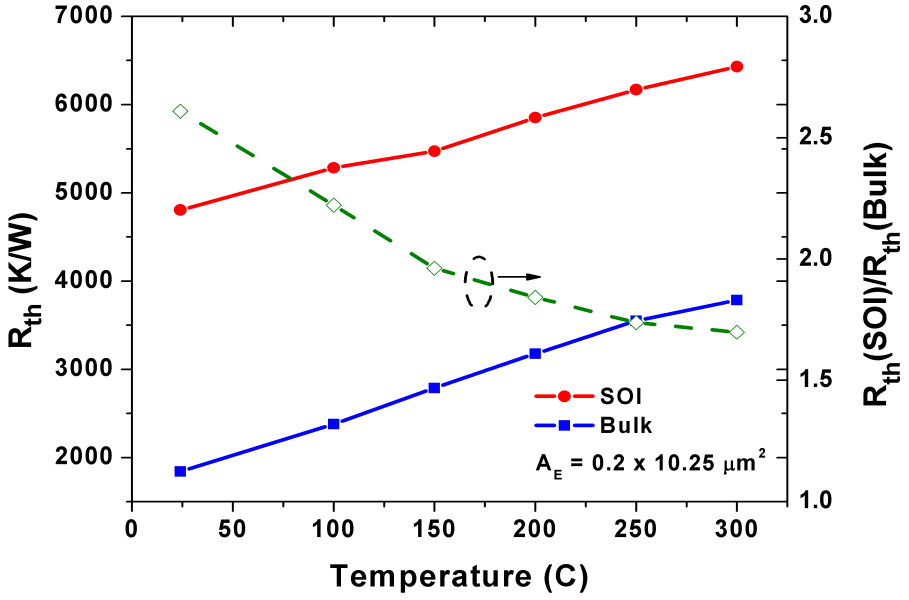
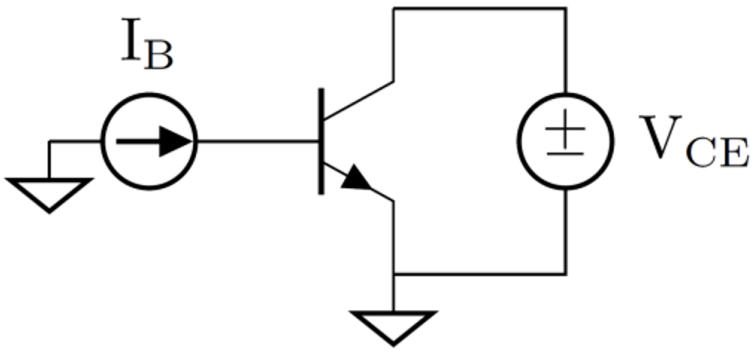


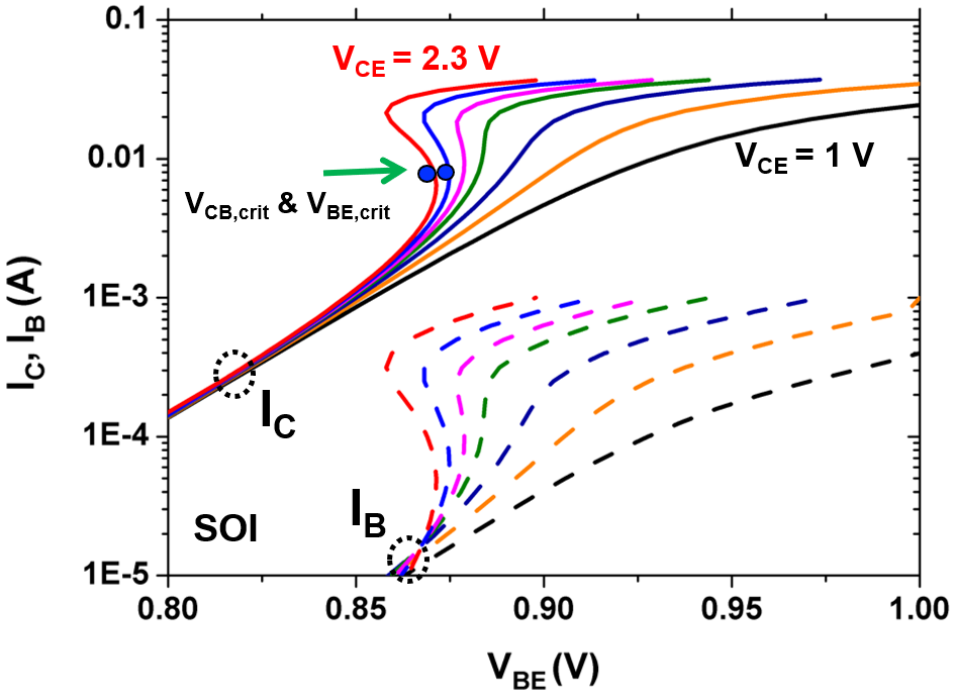
Figure 2.6: Thermal Resistance (R_{th}) as a function of temperature for both bulk and SOI devices with the ratio between SOI and bulk R_{th} overlaid.

Using [36] as the reference, the boundary for safe operation without strong electrothermal instability is defined as the point where $\partial V_{BE}/\partial I_C < 0$. This electrothermal instability point was extracted under a forced-I_B Gummel instead of forced-V_{BE} Gummel in order to accurately measure the negative differential resistance (NDR) region. $V_{BE,crit}$ and $V_{CB,crit}$ are defined as the voltages where the onset of thermal runaway is observed. Forced-I_B Gummel with various V_{CE} over the temperature range of interest were measured to capture these critical voltage points. This setup is highlighted in Fig. 2.7(a), and the NDR region is shown in the Gummel in Fig. 2.7(b).

With increasing temperature, it is expected that $V_{CB,crit}$ should decrease, since higher thermal resistance can potentially cause more self-heating at same DC power, leading to electrothermal instabilities. $V_{BE,crit}$ is expected to naturally decrease since a lower V_{BE} is needed for a fixed I_C with increasing temperature. The measured results plotted in Fig. 2.8, however, indicate a different trend across temperature, especially for $V_{CB,crit}$. The results indicate that for a similar I_C, a higher V_{CB} is needed to initiate the onset of thermal runaway. Up to 150°C, $BV_{CEO} > V_{CB,crit}$,



(a)



(b)

Figure 2.7: (a) Test setup for measuring electrothermally unstable operating conditions. (b) Forced-I_B Gummel with different V_{CE} highlighting the negative differential resistance region.

but past 150°C, the relationship becomes opposite. One of the major implications of this result is that at extremely high temperatures (>150°C), the device is more constrained by BV_{CEO} rather than electrothermal instabilities, which is clearly good news for using SOI in high-temperature applications.

The reason for increasing $V_{CB,crit}$ can be explained by looking at the relationship between $V_{CB,crit}$ and T_{crit} as defined in [37]:

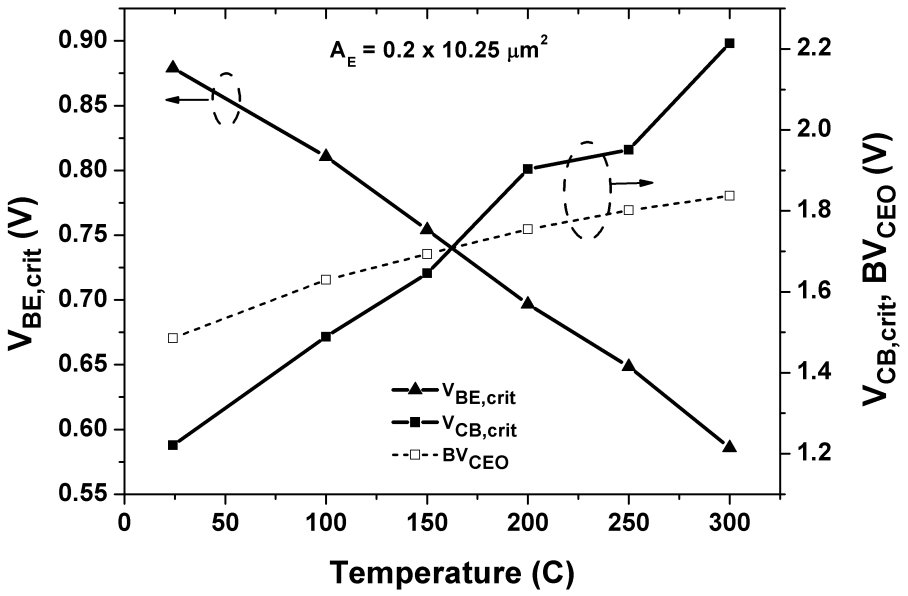


Figure 2.8: $V_{CB,crit}$ and $V_{BE,crit}$ as a function of temperature with the BV_{CEO} overlaid.

$$V_{CB,crit}(J_C) = \frac{\varphi(J_C)\Delta T_{crit}}{\gamma} - \frac{1}{\gamma+1}V_{BE}|_{V_{CB}=0} + \frac{1}{\gamma+1}AJ_CR_{EC} \quad (2.1)$$

where $\varphi(J_C) = \partial V_{BE}/\partial T$, $\gamma = \partial V_{BE}/\partial V_{CB}$ for a fixed I_C, A is the emitter area, J_C is the collector current density, R_{EC} is the series combination of the external emitter and collector resistors, and ΔT_{crit} is defined as:

$$\Delta T_{crit} = \Delta T_{min} + \Delta T_{R,EB} + \Delta T_{R,EC} \quad (2.2)$$

where ΔT_{min} is the change in temperature needed for thermal runaway to occur, $\Delta T_{R,EB}$ is the change in temperature needed to compensate for the decrease in voltage due to base and emitter series resistances, and $\Delta T_{R,EC}$ is the change in temperature needed to compensate for influence of external emitter and collector resistances. The last term in both eq. 2.1 and eq. 2.2 can be neglected here, since the measurement

setup used does not include any ballast resistors. Therefore, eq. 2.1 can be rewritten as:

$$V_{CB,crit}(J_C) = \frac{\varphi(J_C)\Delta T_{crit}}{\gamma} - \frac{1}{\gamma+1}V_{BE}|_{V_{CB}=0} \tag{2.3}$$

While eq. 2.1-2.3 were derived for a SOI Silicon BJT, the underlying concept should still be applicable to these SiGe HBTs. From measured results, γ was found to be negative (ranging from -0.044 to -0.056 over temperature) and $\partial\gamma/\partial T$ was measured as -4.3×10^{-5}. V_{BE} for a fixed I_C at $V_{CB} = 0$ is a decreasing function of temperature, as shown in Fig. 2.2 and the $\partial V_{BE}/\partial T$ and φ at the current density where thermal runaway occurs was measured as -7.9×10^{-4}. The temperature dependent variables in the first term in eq. 2.3 are ΔT_{crit} and γ, while φ is temperature independent [37]. Without any external resistances, ΔT_{crit} is dominated by ΔT_{min}, which is a linear increasing function of temperature. However, as temperature increases, series base and emitter resistances can become significant, which causes an additional increase in ΔT_{crit}, according to eq. 2.2. Overall, this results in the first term of eq. 2.3 increasing with temperature. Both an increasing $|\gamma|$ and $V_{BE}|_{V_{CB}=0}$ should result in the second term of eq. 2.3 to increase. However, it is mostly dominated by $V_{BE}|_{V_{CB}=0}$, since $\partial V_{BE}/\partial T$ is one order of magnitude larger than $\partial\gamma/\partial T$. Therefore, the first term of eq. 2.3 increases with temperature while the second term decreases with temperature, resulting in an overall increasing function of temperature. This temperature dependence for $V_{CB,crit}$ is consistent with the measured results in Fig. 2.8.

2.2.3 AC Characteristics

To accurately measure the peak f_T and f_{max} of the device at high V_{CE} and not run into thermal runaway issues, the forced-I_B method in [36] was used. Both measured h_{21} and MUG showed a nearly ideal 20 dB/dec slope and were reliably used to extract up to

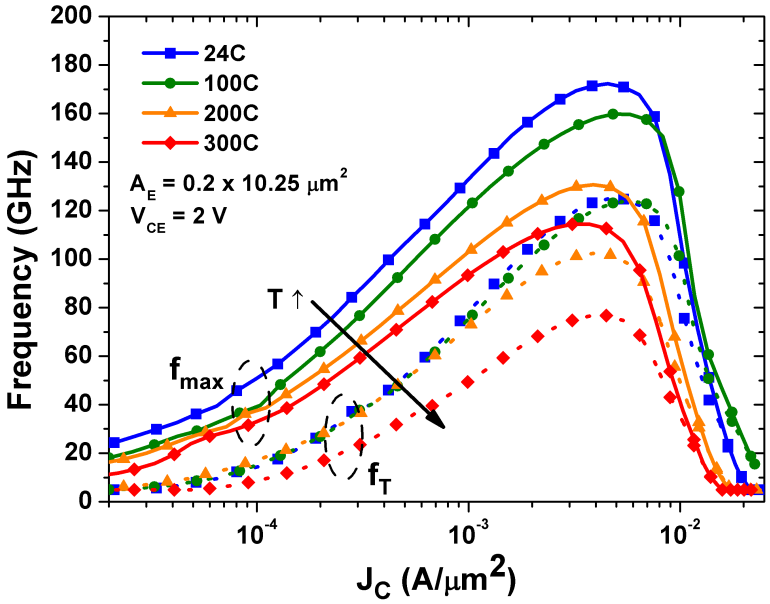


Figure 2.9: f_T and f_{max} as a function of collector current density from 24°C to 300°C for SOI.

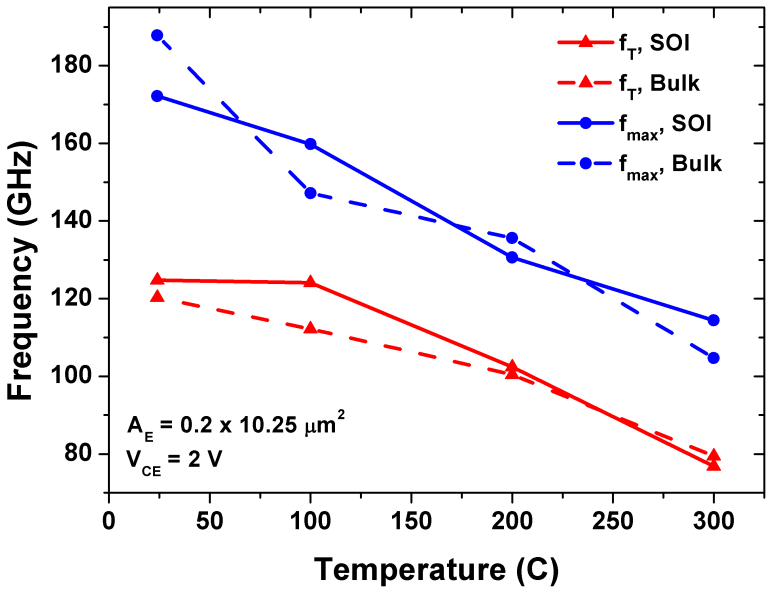


Figure 2.10: Peak f_T and f_{max} as a function of temperature for both bulk and SOI devices.

f_T and f_{max}. Proper deembedding and calibration were obtained at each temperature through the use of calibration substrate standards. V_{CE} of 1.0 V, 1.5 V, 2.0 V were

used for f_T and f_{max} extraction. Fig. 2.9 shows the extracted f_T and f_{max} at 24°C, 100°C, 200°C, and 300°C for a V_{CE} of 2 V as a function of J_C. The V_{CE} of 2 V demonstrated the highest peak f_T and f_{max}. To the best of the author's knowledge, this is the first reported data of measured f_T and f_{max} at 300°C for SiGe HBTs.

A clear decrease in both peak f_T and f_{max} for bulk and SOI devices are observed in Fig. 2.10 with increasing temperature, as expected. For the SOI device, f_T decreases from 125 GHz to 77 GHz (a 38.4% change) while f_{max} decreases from 172 GHz to 114 GHz (a 33.7% change). A similar trend is seen for the bulk devices; however, f_{max} shows a 44% change from 24°C to 300°C. An important observation is that even at 300°C, the device still achieves an $f_{max} > 100$ GHz, more than adequate to support several high-temperature applications. The f_T reduction with temperature can be attributed to the increase in total transit time, which was extracted using [11], and an increasing trend was observed due to enhanced minority carrier scattering in the base, and hence a reduction in mobility. Since f_{max} is directly related to f_T, it also shows a decreasing relationship with temperature. A slight decrease in the $J_{C,Kirk}$ with increasing temperature is also observed in Fig. 2.9 (past 100°C). As $J_{C,Kirk}$ is related to the saturation drift velocity (which decreases with increasing temperature due to higher carrier scattering), $J_{C,Kirk}$ also decreases with increasing temperature, thus reducing the peak f_T and f_{max} at high temperatures [36].

2.3 Summary

DC and AC characteristics, along with thermal effects, were examined from 24°C to 300°C for SiGe HBTs on SOI, and it is demonstrated that high-speed SiGe HBTs on SOI can be operated for most applications even at elevated temperatures as high as 300°C. The next step is to understand how the reliability degradation mechanisms scale with increasing temperature.

CHAPTER 3

RELIABILITY OF SIGE HBTS AT HIGH TEMPERATURES

Extreme environment operation of Silicon-Germanium (SiGe) heterojunction bipolar transistors (HBTs) have been studied extensively in the past due to several inherent advantages they possess. For instance, numerous studies have shown that SiGe HBTs can be operated in both radiation rich environments and at temperature extremes, both low and high [10, 39] . This potentially enables the use of SiGe HBTs in both circuits and large-scale systems that find use in extreme environments. Some examples of SiGe circuits designed and tested for extreme environments can be found in [64, 72–74].

As discussed in the last chapter, SiGe HBTs provide good performance at high temperatures. Even at temperatures up to 300°C, SiGe HBTs demonstrate acceptable performance in key device metrics such as current gain (β), Early voltage (V_A), breakdown voltage (BV_{CEO}), unity gain cutoff frequency (f_T), and maximum oscillation frequency (f_{max}). The realm of high-temperature applications is a rapidly growing field, with some key focus areas including both automotive and aviation electronics [26, 67, 68].

The works reported in [1, 26, 66] examined high-performance SiGe HBTs (aimed at RF applications) operated at high temperatures. However, for some key high-temperature applications, it can be more beneficial to use SiGe HBTs that are optimized for high voltage. This enables the use of SiGe HBTs in applications where

a large voltage drive is required (e.g., drivers) that more frequently encounter high-temperature environments (e.g., in the automotive and aviation sectors). While wide-bandgap semiconductors can be more suitable for these environments, it can be highly cost-effective if silicon-based electronics can be shown to provide sufficient and reliable performance at these high temperatures without any additional shielding or cooling. It is also worth noting that silicon-based technology fabricated on SOI (e.g., C-SiGe on SOI) is also extremely appealing from a high-temperature perspective, since it reduces the off-state susbtrate leakage current, which is one of the more detrimental effects associated with operating silicon-based devices at elevated temperatures.

A serious concern when operating any device in extreme environments is the effect it has on the overall device reliability. Extensive work has been performed on the reliability of SiGe HBTs in radiation-rich environments, from both a total dose and transient response perspective. From a temperature point of view, the electrical reliability of SiGe HBTs at cryogenic temperatures has been reported briefly in [75]. Reliability at high temperatures (>150°C) has been examined briefly in the literature but only in the context of mixed-mode stress [26]. When assessing the reliability of any device, there are several regions of operation that require consideration in order to fully map out the safe-operating-area (SOA) of a given device technology. Aside from electrical reliability, it is also vital to address the electrothermal limitations arising from device self-heating while operating at high powers. The chapter investigates the role of operating temperature on both SOA limits and reliability degradation, in a high-voltage C-SiGe on SOI platform.

3.1 SOA Mapping

As mentioned in Chapter 1, mapping out the SOA trends for any device technology requires precise identification of the key reliability degradation mechanisms and their corresponding failure regions. A sample SOA map is shown again in Fig. 3.1 for

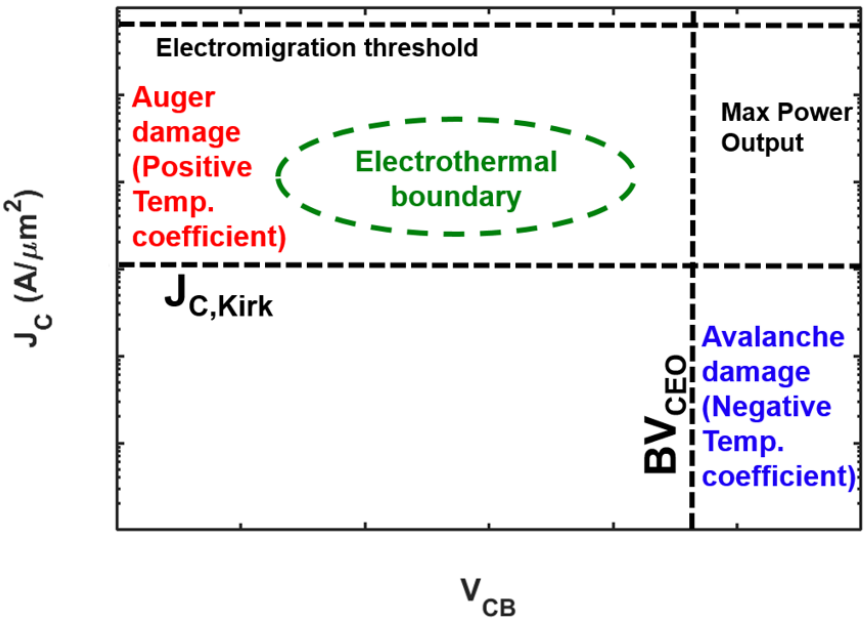


Figure 3.1: General SOA map highlighting the J_C-V_{CB} plane for SiGe HBTs along with the different reliability degradation regions and operative damage mechanisms.

reference. There are two electrical and one electrothermal degradation mechanisms that will be explored in the following sections.

In order to test the two electrical degradation mechanisms, Auger damage and avalanche damage, a mixed-mode stressing approach will be used [76]. The test setup for this measurement is shown in Fig. 3.2. The device is operated in a common-base configuration while the V_{CB} and J_E are independently controlled. This particular stressing approach is useful as it is ideal for traversing the entire output plane since the voltage and currents can be set independently. Therefore, different regions (high voltage and low current or low voltage and high current etc.) can be explored separately.

The devices are stressed with a given V_{CB} and J_E for a given period of time (10,000 s for the purposes of this work), and periodically interrupted to check the "health" of the device. The metric used to check the "health" of the device is the

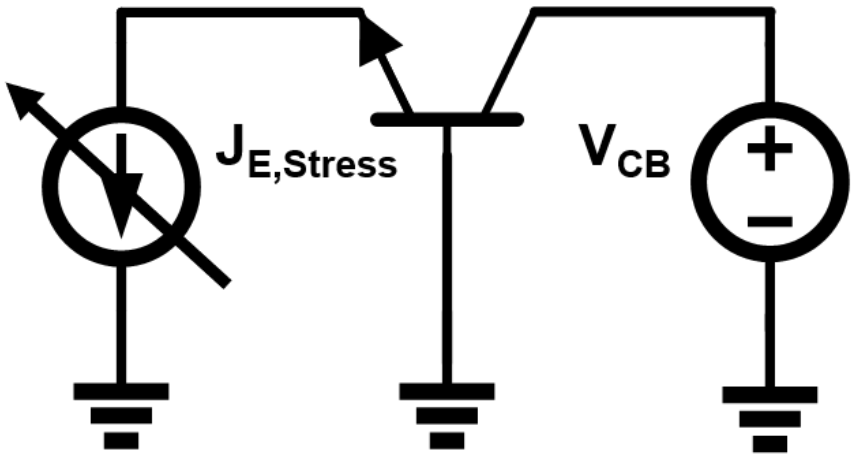


Figure 3.2: Common-base setup used for mixed-mode stress measurements.

Table 3.1: Table summarizing the values of key performance metrics for the NPN and PNP SiGe HBT used in this work [77].

Parameter	**NPN**	**PNP**
β	200	230
BV_{CEO}	48 V	-53 V
Peak f_T ($12V_{CB}$)	4.2 GHz	3.0 GHz

base leakage current. This leakage current is extracted through two different measurements: forward Gummel (FG) and inverse Gummel (IG). A sample FG with applied stress is shown in Fig. 3.3. Base current degradation can be observed in the data with increasing time, which is a result of interface traps at the EB spacer. However, this is not the only relevant oxide interface. The STI is also another important oxide that accumulates damage with stress. In order to sample the base leakage current at the STI interface, IG is used. In inverse mode, the device is essentially operated "upside-down". The physical collector becomes the electrical emitter while the physical emitter becomes the electrical collector.

Auger damage and avalanche damage are the two most important electrical degradation mechanism but as highlighted in the previous chapter, electrothermal limitations are a also a big concern. This is especially relevant in an SOI technology since

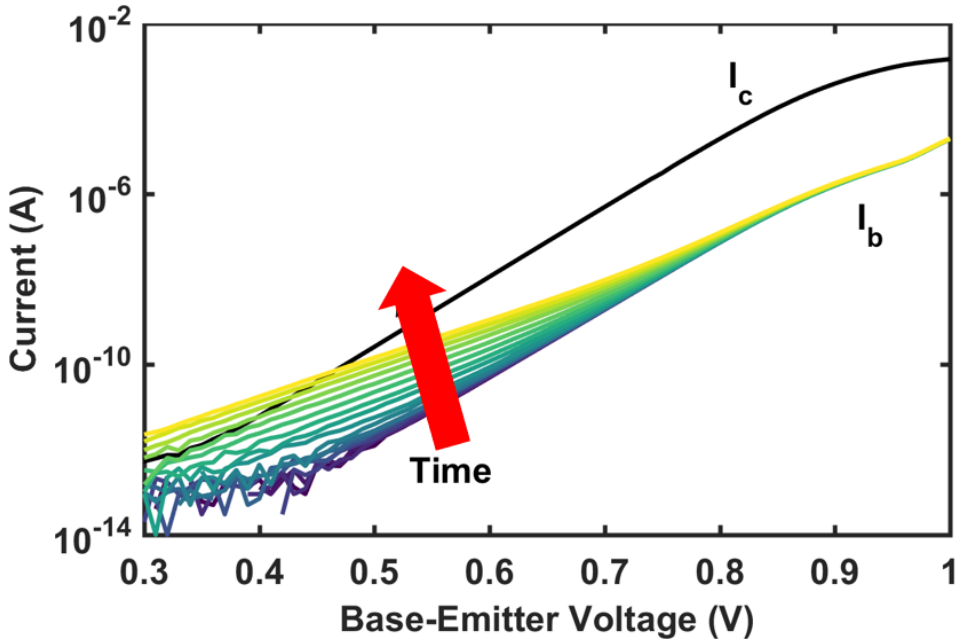


Figure 3.3: Sample FG data with increasing stress time.

the underlying oxide impedes heat flow down to the substrate. A similar measurement setup as Fig. 2.7(a) is used to extract the critical electrothermal operating conditions.

The thermal resistance of any device is one way to quantify its intrinsic thermal properties. Thermal resistance data across temperature was reported in [1, 26, 66]. Some work for the electrothermal behavior of SiGe HBTs across temperature has been investigated in [1] as shown in the previous chapter; however, that work only examined the electrothermal behavior for a single collector current density and not across the whole SOA region.

3.2 Technology and Measurement Details

The devices used in this work are from a 36 V complementary SiGe HBT on SOI platform [77]. The NPN and PNP SiGe HBTs are built on top of a 0.4 μm SOI oxide, while being optimized for a high β-V_A product. Relevant device metrics for both the NPN and PNP are listed in Table. 3.1. It should be highlighted that these devices are not meant for RF applications like for most modern SiGe HBTs, and are optimized for high-performance and high-voltage analog applications. This obviously

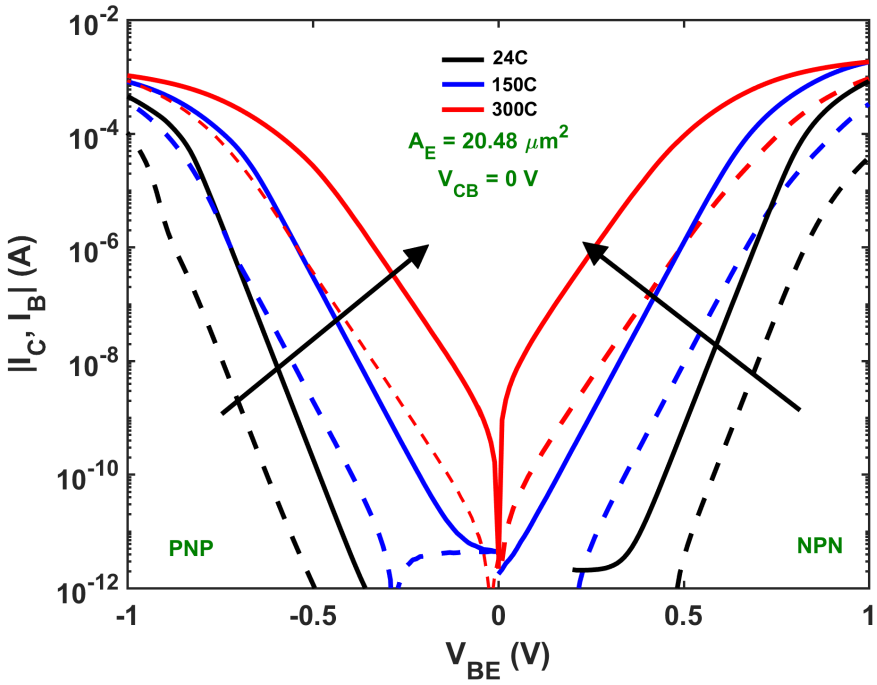


Figure 3.4: Forward Gummel plots for both NPN and PNP SiGe HBTs across temperature from 24°C to 300°C. Solid lines are I_C and dotted lines are I_B.

has important implications from both a device performance and reliability perspective due to the significant doping and structural changes needed to accommodate higher voltage operation.

All measurements presented were performed on-wafer using a high temperature hot chuck capable of temperatures up to 300°C. High temperatures DC probes were used to make both characterization and stress measurements. An Agilent 4155 was used as the main measuring and stressing equipment. In order to get the best measurements at each temperature, the die was left undisturbed for 15 minutes once the set temperature was reached to achieve thermal equilibrium. The probes were also probed down during this time so that the probes would be at the same temperature as the die. All devices used in this work have a device geometry of 0.4 x 25.6 x 2 μm^2.

Some characterization measurements were performed on devices up to 300°C to explore their high-temperature DC performance. Fig. 3.4 shows the forward Gummel

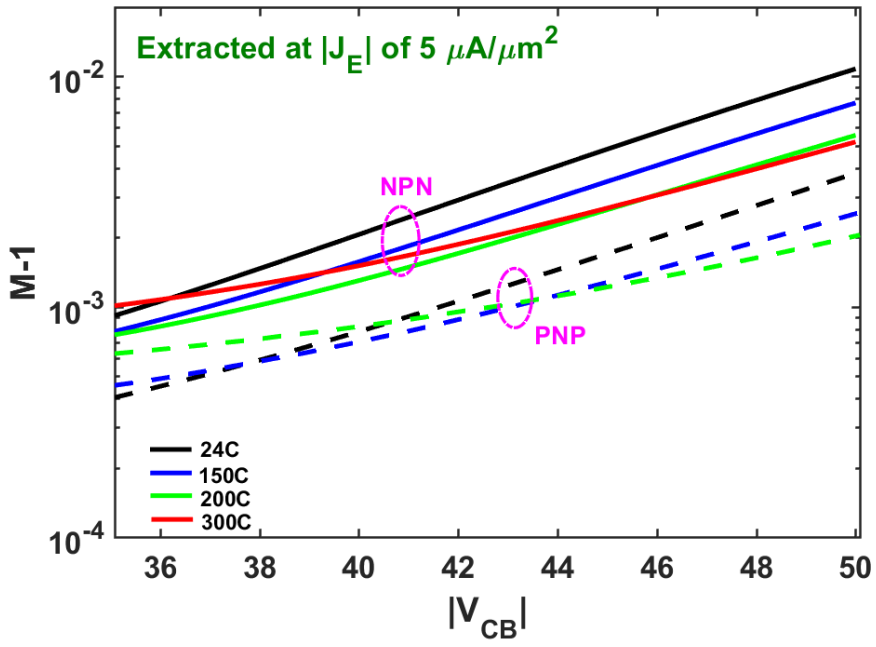


Figure 3.5: Impact ionization for both NPN and PNP devices across temperature from 24°C to 300°C. Solid lines correspond to the NPN devices and dotted lines correspond to the PNP devices.

characteristics for both the NPN and PNP SiGe HBTs. Both types of devices illustrate classical Gummel characteristics with increasing temperature, and a decrease in the slope (or transconductance) is observed with rising temperature. While not shown here, the measured current gain decreases monotonically with increasing temperature, with a maximum reduction of approximately 25%, which is consistent with measured results in the literature [1, 26]. M-1 data across temperature for both NPN and PNP SiGe HBTs are illustrated in Fig. 3.5. Both NPN and PNP devices exhibit a decreasing M-1 with increasing temperature, as expected, which acts to increase BV_{CEO} and thus extend the SOA.

3.3 Stress Measurements

3.3.1 High-Voltage, Low-Current Stress

The first SOA region that was investigated was the high-voltage, low-current region. To assess the stress degradation, mixed-mode stress, as described in [76], was applied.

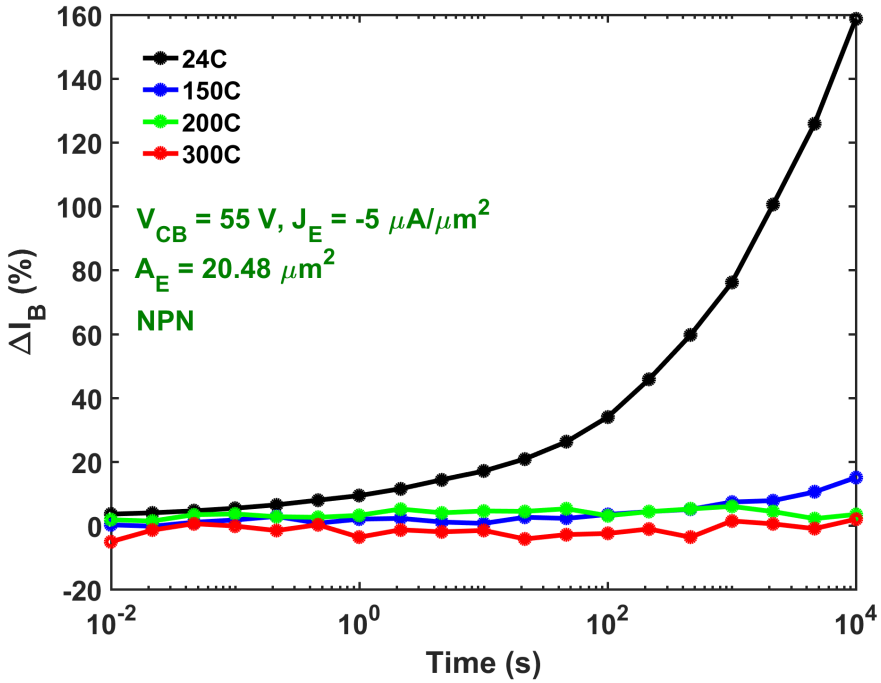


Figure 3.6: Change in inverse Gummel base current in percentage for an NPN SiGe HBT as a function of stress time up to 10,000 s for a stress condition of V_{CB} = 55 V and J_E = 5 μA/μm^2. The different curves correspond to different temperature points. The change in base current is extracted at a J_C of 0.1 μA/μm^2.

A large V_{CB} together with a small J_E was applied as the stress condition. The applied V_{CB} was chosen to be between BV_{CEO} and BV_{CBO}, while the J_E was chosen to be 2-3 orders of magnitude less than peak $J_{C,Kirk}$ in order to avoid Kirk effect, which would complicate the results. All stress conditions were applied for a total of 10,000 seconds to obtain the best long-term trends.

The stress results for one stress condition for both NPN and PNP devices are highlighted in Fig. 3.6 and Fig. 3.7, respectively. This stress condition was selected because it best captured the trends observed across temperature. While only one stress condition is highlighted here, several other stress conditions were also performed (V_{CB} = 54-60 V). This particular stress condition is shown here as it was a good statistical representation of the stress trend. Since the BV_{CEO} increases by up to 6 V over the temperature range of interest, the chosen stress voltages needed to be

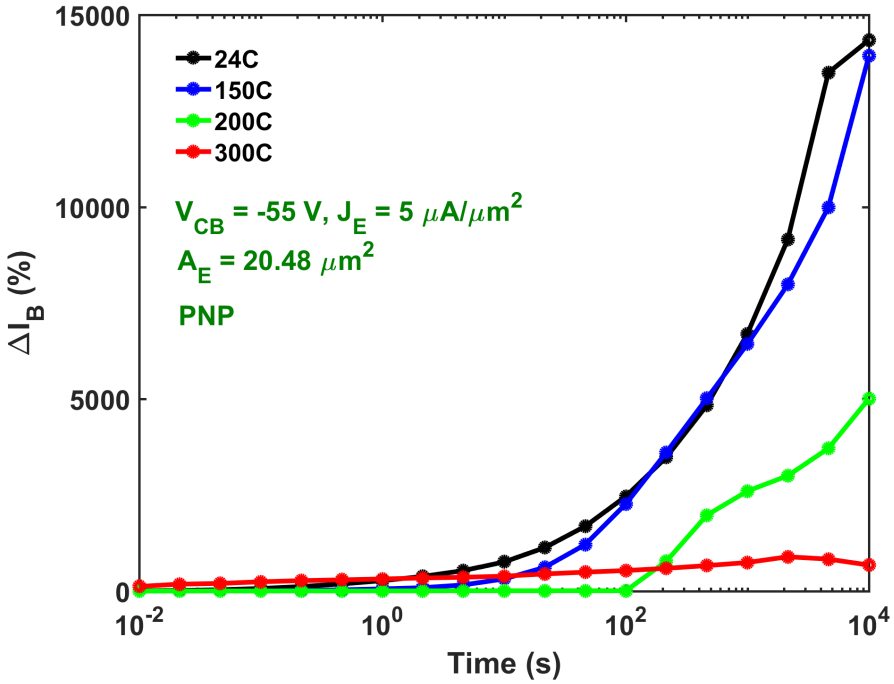


Figure 3.7: Change in inverse Gummel base current in percentage for a PNP SiGe HBT as a function of stress time up to 10,000 s for a stress condition of V_{CB} = -55 V and J_E = -5 μA/μm^2. The different curves correspond to different temperatures. The change in base current is extracted at a J_C of -0.1 μA/μm^2.

high enough to cause mixed-mode damage at every temperature point. In order to quantify the damage, the change in base current in both FG and IG were analyzed.

Fig. 3.6 and Fig. 3.7 illustrate change in base current in percentage from IG with increasing stress time for NPN and PNP, respectively. For both the NPN and PNP devices, the change in base current from FG across temperature is minimal and as such it is not shown in these figures. This is an expected result since the peak electric field is deep within the CB junction and is too far from the EB spacer interface to cause interface damage. This is especially true in this device technology due to the lower collector doping to accommodate for a higher breakdown voltage. Consequentially, this leads to an almost zero temperature dependence from a FG perspective for mixed-mode reliability.

However, the damage is far more emphasized in the IG response as illustrated in

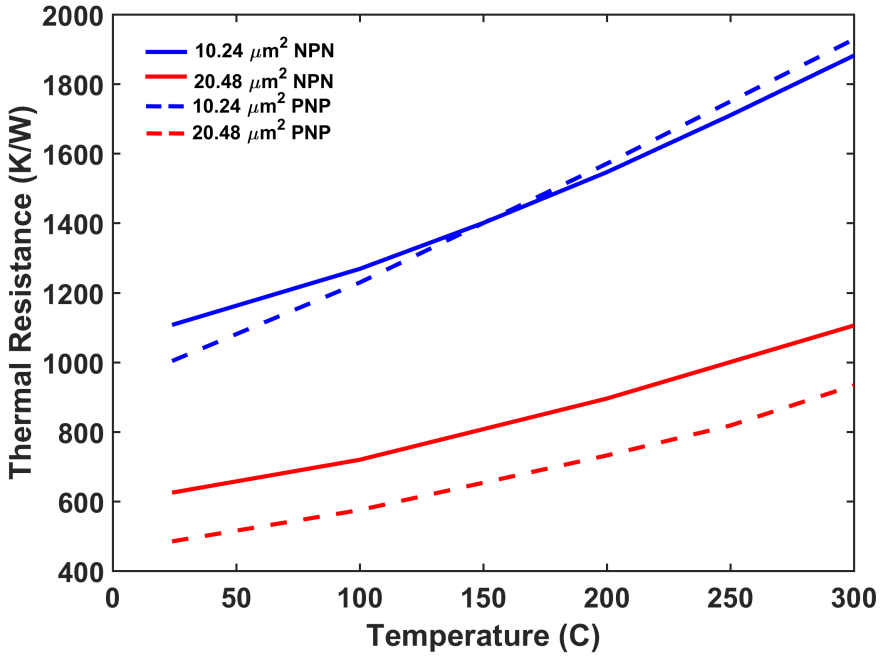


Figure 3.8: Thermal resistance for two different NPN and PNP SiGe HBT geometries across temperature from 24°C to 300°C.

both Fig. 3.6 and Fig. 3.7. This is largely driven by the damage along STI oxide interface. While the peak electric field is too far away from the EB spacer, it is in closer proximity to the STI. This leads to a higher probability of hot carriers generated from the CB junction reaching the STI interface. It should be noted that there is a significant difference in total damage between the NPN and PNP devices. Fig. 3.5 already illustrated that M-1 should be lower for the PNP device relative to NPN device so the mixed-mode damage should not be so high for PNP devices. One possible reason for this discrepancy was explored in [78] where differences in the activation energy for the damage between oxide interfaces in NPN and PNP devices leads to PNP devices exhibiting more damage for a similar stress condition than NPN devices. The temperature dependence, however, shows a clear negative temperature coefficient. Similar to what was reported in [2], mixed-mode stress illustrated a slight degradation in the high current behavior due to collector resistance increase for both NPN and PNP devices. Overall, at temperatures as high as 300°C, the damage

reduction is massive relative to the 24°C results. From an SOA perspective, this is a desirable trend as the maximum operable voltage increases.

3.3.2 Electrothermal Boundary

The intrinsic thermal behavior of SiGe HBTs can be quantified through thermal resistance measurements which was extracted using the method in [71]. The results for both NPN and PNP devices of two different geometries are indicated in Fig. 3.8 where the thermal resistance is plotted as a function of temperature from 24°C to 300°C. For both NPN and PNP devices, the trend is similar where an almost linear positive temperature coefficient is observed. Another key observation is the difference in thermal resistance between single emitter finger devices and multiple emitter finger devices. Similar to previous work in [26], multiple emitter finger devices show significantly smaller thermal resistance relative to single emitter finger devices and this trend is consistent across the entire temperature range.

While thermal resistance measurements are a good quantitative measurement for compact modeling purposes and to extract internal junction temperature, it does not translate directly to the SOA from an electrothermal perspective. In order to quantify the electrothermal boundary of the devices used in this work, a similar approach to [36] is used. Essentially, a forced-I_B Gummel approach was used to quantify critical voltage and current values. Using a forced-I_B Gummel instead of a forced-V_{BE} Gummel enables measurement of the device characteristics at very high DC power (>100 mW) without catastrophically burning out the device due to thermal runaway. In this work, the electro-thermal boundary is defined as the point where $\partial I_C/\partial V_{BE} < 0$. For each forced-$I_B$ Gummel measurement, a constant V_{CE} is used. Measurements are then subsequently made across the entire V_{CE} operation region to obtain the critical voltage and current points across the J_C-V_{CB} plane.

$V_{CB,crit}$ and $J_{C,crit}$ are extracted from the forced-I_B measurements for both the

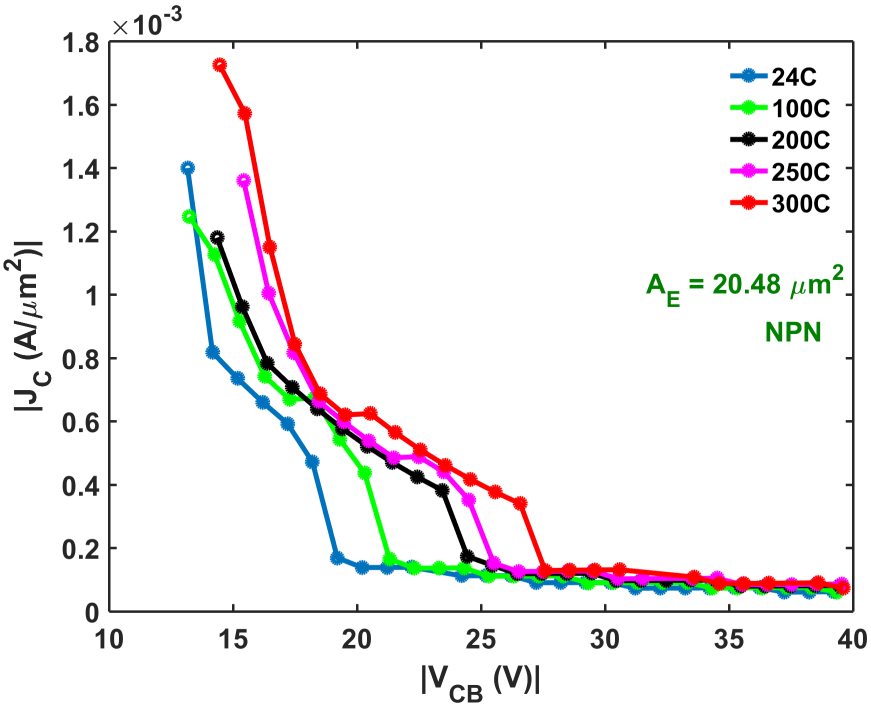


Figure 3.9: Electrothermal boundary for an NPN device that highlights the critical J_C and V_{CB} across temperature from 24°C to 300°C.

NPN and PNP devices and the results are illustrated in Fig. 3.9 and Fig. 3.10. The first $V_{CB,crit}$ point is the V_{CB} value at which the electro-thermal instability point is observed. The plots do not begin at earlier V_{CB} values because the forced-I_B Gummel do not exhibit any electro-thermal instability through the entire swept I_B values (i.e V_{BE} up to 1 V). Thus, it can be said that the electrothermal constraints are only evident past a certain V_{CB} threshold.

The NPN electrothermal boundary in Fig. 3.9 illustrates an interesting overall trend. First, for each temperature, it can be seen that there is an initial region where there is a relatively steep shrinkage in the maximum allowable J_C with increasing V_{CB}. This is the first limiting region in the electrothermal boundary. The second region of importance is the relatively flat region at higher V_{CB}. This second region essentially sets the upper limit on the allowable J_C past the initial region. One of the main implications of the trend in this region is that even with the larger V_{CB}

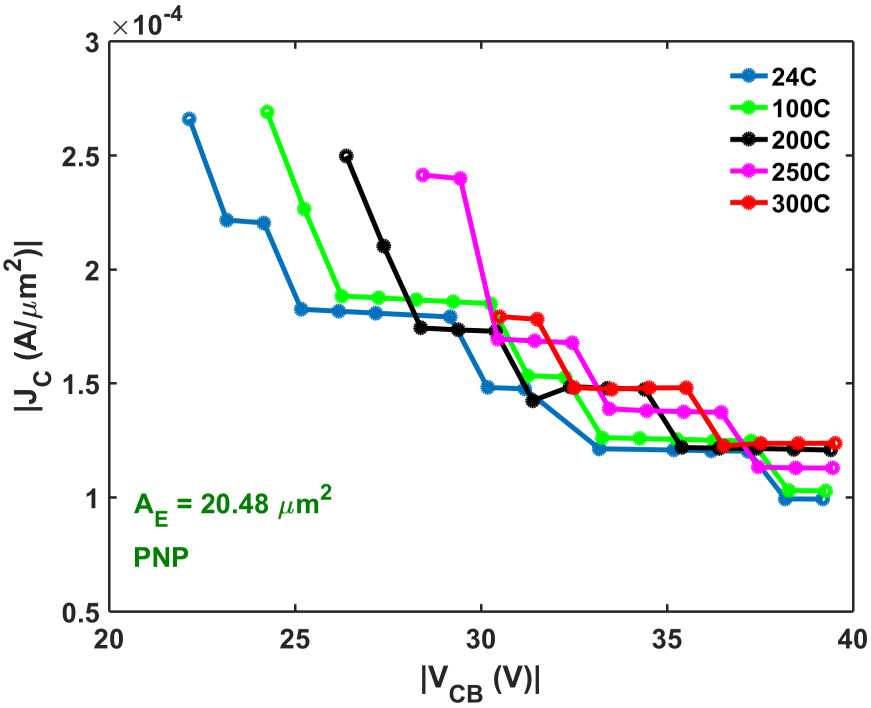


Figure 3.10: Electrothermal boundary for a PNP device that highlights the critical J_C and V_{CB} across temperature from 24°C to 300°C.

increasing the total power dissipation, it does not necessarily decrease the maximum allowable current drastically to shrink the SOA. However, it is worth pointing out that the electrothermal boundary does start approaching the $J_{C,Kirk}$ ($\approx 100\ \mu A/\mu m^2$ at a V_{CB} of 20 V) value at large V_{CB}. This obviously has implications on device speed and performance at large V_{CB} values as the AC performance and gain will degrade sharply.

From an over-temperature perspective, with increasing temperature, the electrothermal boundary starts to extend the SOA. This trend is highlighted in Fig. 3.9 where with each successive temperature curve, the electrothermal boundary shows a clear shift to the right and thus enabling a higher maximum V_{CB} for a constant J_C. This trend is more clearly visible in the first region discussed previously. While the SOA does extend outwards, there is some saturation in certain regions of the SOA. From about 20-30 V, a much more significant extension of the SOA is observed relative

to the 15-20 V range. The final region at very large V_{CB} shows almost no temperature dependence which indicates that this region is likely limited by the maximum power output.

The PNP device electrothermal boundary illustrated in Fig. 3.10 shows a similar overall trend as the NPN device but with some key differences in the shape of the curve. Unlike the NPN device, there is no saturation observed at high V_{CB}. The data indicates an almost linear boundary across the J_C-V_{CB} plane. Another key difference observed between the NPN and PNP device is the drastic change in initial V_{CB} at which thermal instability is observed. At 24°C, $V_{CB,crit}$ happens at approximately 22 V while at higher temperatures, it shifts significantly to the right with 300°C showing an initial V_{CB} of 30 V. This is obviously an extremely desirable trend since it allows for a much higher operable voltage for a given current with increasing temperature relative to the NPN device. However, it is worth noting that unlike the NPN device, the PNP device sources and sinks much less peak current (approximately one order of magnitude difference). For certain applications, this could make PNP devices more desirable than NPN devices.

The presented results show a temperature dependence that is somewhat in conflict with the temperature trend observed for the thermal resistance. Thermal resistance measurements across temperature indicate that with increasing temperature, the internal device temperature should increase significantly for a constant dissipated power as given by:

$$\Delta T = T_j - T_{amb} = P_{diss} R_{TH} \tag{3.1}$$

where T_j is the junction temperature, T_{amb} is the ambient temperature, P_{diss} is the dissipated power, and R_{TH} is the thermal resistance. This was looked at in more detail in [1] where it was shown that the internal temperature increase needed to cause thermal runaway increases with increasing temperature which is consistent with

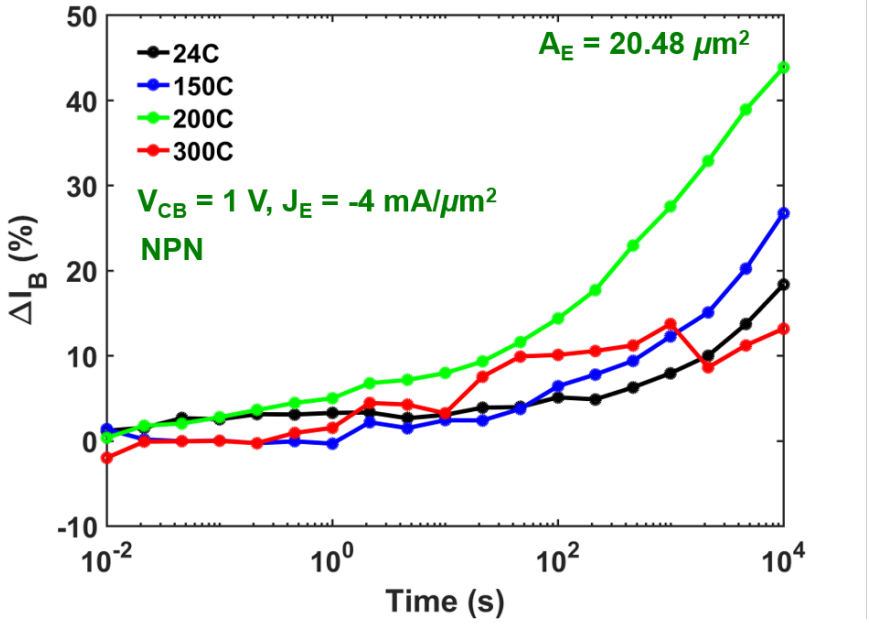
the results shown here.

3.3.3 High-Current, Low-Voltage Stress

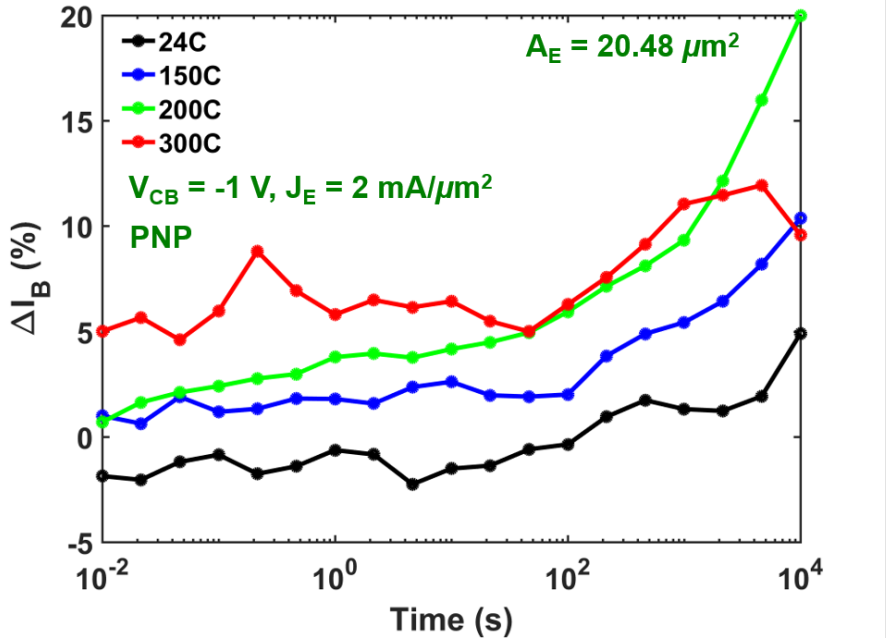
Similar to the mixed-mode stress measurements, a common-base configuration was used to stress the devices with a fixed J_E and V_{CB}. The stress conditions were chosen to maximize Auger damage and minimize mixed-mode induced damage. J_E values were slowly increased from above $J_{C,Kirk}$ up to a point where damage was observed. For each J_E value, different V_{CB} values were also applied to better understand the V_{CB} dependence for Auger induced damage.

The high-current stress results for both NPN and PNP devices at a low V_{CB} are illustrated in Fig. 3.11 across temperature. Fig. 3.11(a) shows the stress results for an NPN device while Fig. 3.11(b) shows the stress results for a PNP device. The plots illustrate the change in base current from IG in percentage as a function of stress time. While only the base current change from IG is shown, the results indicated a similar trend from FG extraction. The key difference is that the FG extracted base current change is generally on a smaller magnitude than the IG extraction so the IG change in base current was plotted to more clearly illustrate the observed trends. Only two stress conditions are shown for each NPN and PNP devices just to highlight the primary trends.

It should be noted that the applied J_E for the NPN device is 4 mA/μm^2 while for the PNP device it is -2 mA/μm^2. This was mainly chosen to better highlight the trends and differences between the NPN and PNP. For both NPN and PNP devices at low V_{CB} in Fig. 3.11(a) and Fig. 3.11(b), an expected trend is observed up to 200°C, where the the damage increases monotonically which is consistent with the Auger damage physics [35]. For the NPN device, from 24°C to 200°C, there is approximately a 2x increase in base current after 10,000 s while for the PNP device, there is approximately a 4x increase in base current after 10,000 s. Interestingly



(a)



(b)

Figure 3.11: Change in inverse Gummel base current in percentage for (a) an NPN device as a function of stress time up to 10,000 s for a stress condition of V_{CB} = 1 V and J_E = 4 mA/μm^2, (b) a PNP device as a function of stress time up to 10,000 s for a stress condition of V_{CB} = -1 V and J_E = -2 mA/μm^2. The different curves correspond to different temperature points. The change in base current is extracted at a $|J_C|$ of 0.1 μA/μm^2 for all plots.

enough, an unexpected trend is observed at 300°C for both the NPN and PNP devices. For the NPN device in Fig. 3.11(a), the damage with stress time for the 300°C case is actually lower than the 200°C case. As the stress time approaches 10,000 s, some annealing is even observed. This annealing trend is additionally observed in the PNP device too in Fig. 3.11(b).

This reduction in damage at 300°C is inconsistent with the temperature dependence of Auger physics. However, it can be explained by understanding the damage creation process. As damage is created by hot carriers reaching the Si/SiO_2 interface, there is an additional reverse reaction worth considering. The following equation from the reaction-diffusion model for interface trap density (N_{it}) is defined as [35]:

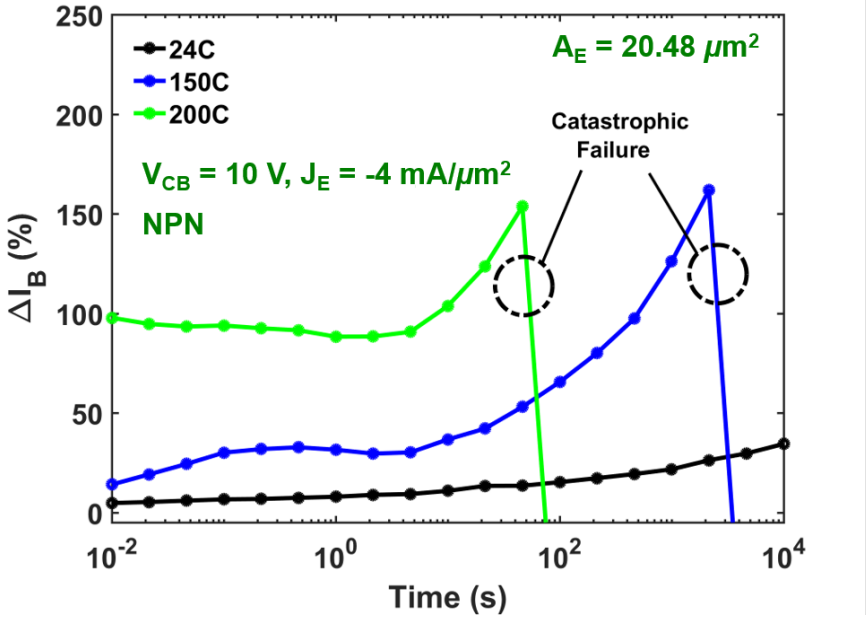
$$\frac{\partial N_{it}}{\partial t} = K_F(N_0 - N_{it}) - K_R N_{it} H_2 \tag{3.2}$$

where K_F and K_R are the forward and reverse reaction rate, respectively, and N_0 and H_2 are the dangling bond density at the interface and the hydrogen density at the interface, respectively. K_F is driven largely by the hot carrier generation rate which in this case is dictated by the Auger recombination rate. The measured Auger recombination rate, in particular, is known to increase at least up to 150°C for n-type silicon [79]. The measured results up to 200°C here indicate that this positive temperature coefficient, at the very least, extends up to this temperature range. It should additionally be noted that K_F is also a function of the Auger recombination energy distribution function (EDF), which has a clear positive temperature coefficient due to the thermalized energy tail [35]. The reverse reaction is essentially an annealing reaction dominated by the diffusion of hydrogen to the dangling silicon bonds at the interface. This is known to increase with temperature due to an increase in the hydrogen diffusion rate with increasing temperature [80, 81].

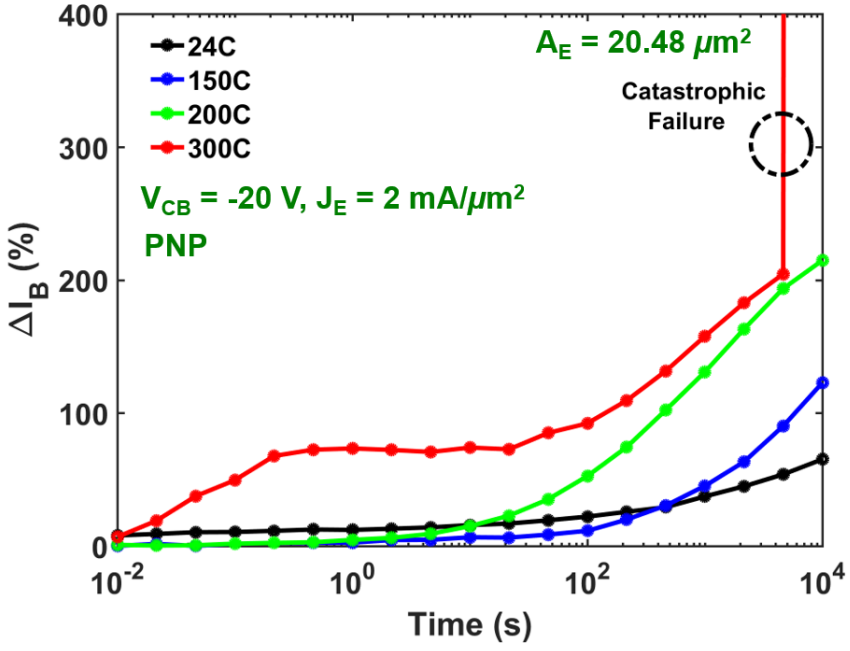
At temperatures as high as 300°C, it very likely that the reverse reaction (i.e.

annealing) dominates the overall reaction leading to a suppression in the total damage as observed in Fig. 3.11(a) and Fig. 3.11(b). A major conclusion that can be drawn from this behavior is that there exists a range of temperatures within 200°C-300°C where the annealing reaction is comparable or even greater than the forward reaction (Auger recombination). Identifying such a temperature range has beneficial implications for the SOA since it means that high-current operation will not be as detrimental as one might expect for really high temperatures (>200°C).

The effect of higher V_{CB} on this damage mechanism was also investigated and the results are indicated in Fig. 3.12(a) and Fig. 3.12(b) for the NPN and PNP devices, respectively. For both NPN and PNP devices, the ΔI_B is more than 20-100x larger with a higher V_{CB} stress across all temperature points. These results indicate that with enough self-heating, the damage does increase significantly which leads to the conclusion that the Auger recombination rate still dominates at very high internal temperature ($T_J > 300$°C). It should be noted, however, that catastrophic failure is observed in both cases in Fig. 3.12(a) and Fig. 3.12(b). The NPN starts to show catastrophic failure at temperatures as early as 150°C while the PNP device shows catastrophic failure at 300°C. There is no stress curve shown for the NPN at 300°C as it failed instantly with stress. When stressing these devices at the high-current and high-voltage regime, there is also an interplay of electrothermal effects that have to be considered which is likely helping cause catastrophic failures. Through all the stress conditions that we measured (including ones not shown here), the NPN devices in general showed catastrophic failure at earlier temperature conditions and at lower V_{CB} values than the PNP devices. This result is consistent with the trend observed in the previous section where the PNP devices were more robust from an electrothermal perspective to larger V_{CB} than the NPN devices. The larger R_{TH} observed for the NPN relative to the PNP as shown in Fig. 3.8 also helps explain the more frequent catastrophic failures observed for this particular NPN device geometry as it has 25%



(a)



(b)

Figure 3.12: Change in inverse Gummel base current in percentage for (a) an NPN device as a function of stress time up to 10,000 s for a stress condition of V_{CB} = 10 V and J_E = 4 mA/μm^2, (b) a PNP device as a function of stress time up to 10,000 s for a stress condition of V_{CB} = -20 V and J_E = -2 mA/μm^2. The different curves correspond to different temperature points. The change in base current is extracted at a $|J_C|$ of 0.1 μA/μm^2 for all plots.

Figure 3.13: Metal test structure for accelerated electromigration testing.

higher R_{TH} across the whole temperature range.

3.4 Electromigration

While not a device-related reliability concern, electromigration is an important degradation mechanism at elevated temperatures [16]. Especially for temperatures >200°C, electromigration is a huge concern, and there are almost no reported electromigration data in literature at these temperatures. In order to perform accelerated electromigration testing, the structure shown in Fig. 3.13 was used. The smallest feature size of the technology platform was used, which was 0.5 μm in this case, to perform the most efficient stress testing. The total length of the test line was approximately 1 mm. Kelvin taps were implemented on the structure so that current is forced through one path while voltage is measured on the other for accurate resistance measurements. In order to prevent electromigration failure at or near the pads, the metal line was split into three branches to reduce the current density. The particular technology platform used in this work contained three metal layers each using the same metal, therefore three separate but identical structures were used.

The general testing procedure consisted of forcing a set current density across the metal line, and measuring the voltage across the line. In doing so, one is able to constantly measure the resistance based on Ohm's law. A metal was considered to fail if the resistance exceeded its nominal value by 50%. The results for temperatures >200°C is shown in Fig. 3.14. M1 is the bottom-most metal line (closest to device) while M3 is the top-most metal line (closest to top of wafer). A stress current density of 10 mA/μm^2 was used for all temperatures. A sample size of three metal lines

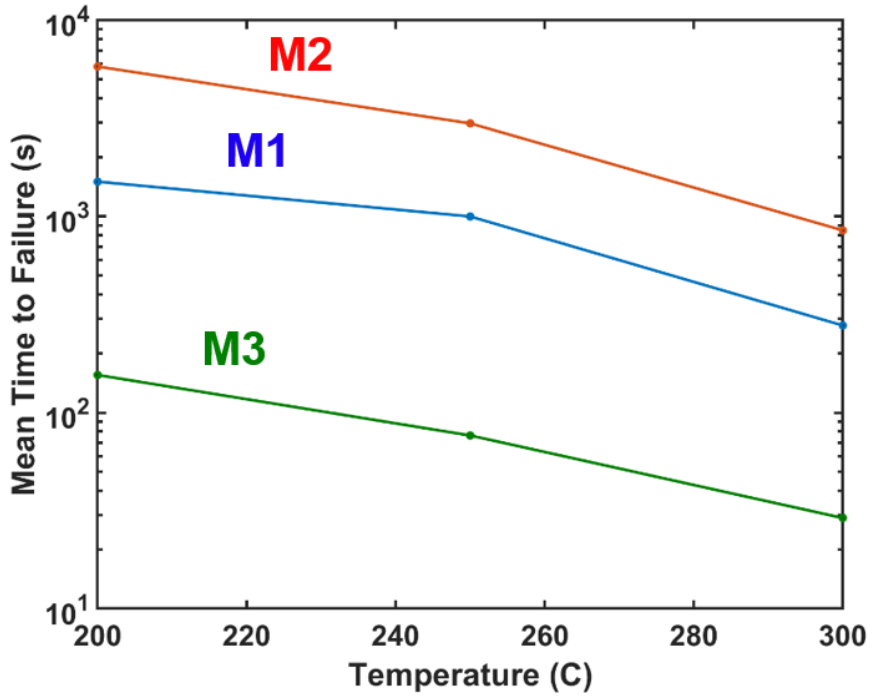


Figure 3.14: Mean time to failure as a function of temperature for three different metal layers. A stress current density of 10 mA/μm^2 was used.

were used and their MTTF was averaged for each data point. As expected based on Black's equation, a strong reduction (almost linear on log scale) in the MTTF is observed. While it is not possible to get a statistical representation of the MTTF based on the small sample size used here, it still provides insight into the expected degradation one can expect for metal lines at these high temperatures.

An interesting, non-monotonic trend is also observed across the metal lines, where M3 shows the worst MTTF and M2 shows the best MTTF. There are two possible reasons for this. One is the sample size is too small and that the results could potentially be skewed by outliers. Another possible reason is the heat flow distance. It is easier for majority of the heat flow to conduct downwards to the substrate since the bottom of the wafer is directly in contact with the hot chuck. Heat can also flow upwards but it is much harder for heat to conduct through air at the top. Therefore, M3 can be said to have the largest thermal resistance since it is farthest from the

substrate. M2 likely has the lowest thermal resistance since it is close to both the substrate and the top while M1 has a slightly higher thermal resistance since it is close to the substrate but much further from the top. A larger sample size is required to make any conclusive statement on this trend. However, the key conclusion from the measured results is that metal lines for high-temperature applications should be significantly wider than required for room temperature applications to mitigate electromigration.

3.5 Summary

The SOA trends for a complementary SiGe-on-SOI technology was explored up to 300°C. Device level reliability measurement results were shown for different device bias regions. The SOA trends across temperature are summarized in Fig. 3.15. Mixed-mode stress illustrates a negative temperature coefficient that bodes well for high-temperature applications that require large voltage swing where a larger voltage swing than conventionally defined BV_{CEO} will be possible. As this is a SiGe-on-SOI device, self-heating induced electrothermal instability also plays a large role in the SOA. The critical J_C and V_{CB} were mapped out along the J_C-V_{CB} plane. The electrothermal boundary was shown to increase for both the NPN and PNP with increasing temperature which implies that with increasing temperature, there is a larger margin of operation for maximum dissipated power before reaching an electrothermally unstable operation point. It should be noted that these measurements were for a DC condition and there should potentially be a larger extension of the SOA when looking at more of a pulsed, circuit type operation.

The high-current, low-voltage region was also looked at across temperature and the Auger damage in this region exhibited a positive temperature coefficient. This has major implications on the high-current circuit operation of SiGe HBTs at higher

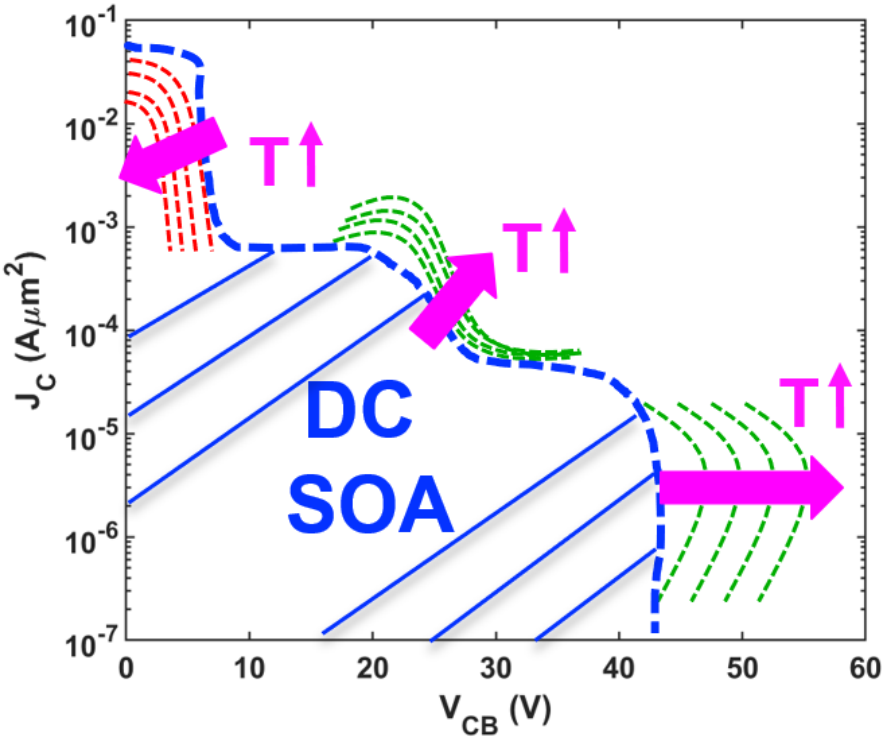


Figure 3.15: High-level summary of the key SOA shifts with increasing temperature.

temperatures (up to 200°C). However, it was seen that at 300°C operation, the high-current induced damage reduced and illustrated an annealing behavior which implies that there is a temperature range where annealing dominates over Auger damage and thus slightly extends the SOA for high temperature operation. Electromigration was also briefly explored, and a strong reduction in metal reliability was measured. Therefore, wide metal lines are highly recommended for high-temperature circuit desing. Overall, SiGe HBTs on SOI illustrate a lot of favorable high-temperature behavior which can potentially enable the use of SiGe HBTs in high-temperature applications.

CHAPTER 4

BUILDING HIGH-TEMPERATURE CAPABLE ANALOG CIRCUIT BUILDING BLOCKS USING SIGE HBTS

High-temperature electronics have garnered increasing attention in recent years due to the emerging markets in aviation, automotive, and energy exploration (oil, gas, etc.) [1, 67]. In principle, wide-bandgap semiconductors such as GaN and SiC are better-suited for high-temperature environments ($> 200°C$), since bulk silicon-based devices exhibit severe leakage current at these temperatures. However, while these wide-bandgap semiconductors are more suitable from a performance perspective, it would still be ideal to be able to use silicon-based designs, due to their inherently lower cost, higher yield, ease of manufacturing, high reliability, and easier integration with CMOS control electronics. Key to any Si-based approach is to use silicon-on-SOI technology to reduce substrate leakage current, which makes it easier to build large circuits capable of operating at elevated temperatures for long periods of time.

Operation of silicon-germanium heterojunction bipolar transistors (SiGe HBTs) at high temperatures has been an area of recent interest due to its favorable DC and AC performance, even at temperatures as high as 300°C [1, 26, 66]. Current gains (β) over 100, and f_T/f_{max} over 100 GHz at 300°C have been demonstrated in previous work, which position SiGe HBTs as an enabling technology for circuits operating at these extreme temperatures [1]. However, long-term reliability at high temperatures is a valid concern. Reliability of SiGe HBTs at temperatures up to 300°C was reported in [2] and discussed in the previous chapter. The results indicated that SiGe HBTs can be operated at these extreme temperatures without substantial degradation. Suppression of classical mixed-mode stress at 300°C was observed, along

with favorable electrothermal behavior, which bodes well for long-term operation of SiGe HBTs at high temperatures.

To date, the bulk of the literature in this field has only examined device-level operation of SiGe HBTs at high temperatures. The work in [82] showed design and operation of a SiGe BGR circuit using a bulk SiGe HBT technology. However, there have been no reported results of high-temperature circuit design using SiGe-on-SOI HBT technologies. In this chapter, the design and operation of basic analog building block circuits for high-temperature operation using a complementary SiGe-on-SOI HBT (C-SiGe-on-SOI HBT) technology is reported. In particular, a current mirror, a BGR, and a class-AB push-pull output stage were designed and measured up to 300°C using calibrated compact models. A preliminary assessment of their robustness for long-term operation in such environments was also made. A simple method for calibrating compact models for use at high temperatures is also discussed.

4.1 Technology and Measurement Details

This work utilizes a high-voltage (> 30 V) C-SiGe-on-SOI HBT platform [77]. Since these devices are optimized for high-voltage analog applications, they are not intended for RF operation. Therefore, simple analog building block circuits were chosen to best illustrate the viability of using SiGe-on-SOI HBTs at high-temperatures. All circuits shown in this work only use NPN and PNP devices. Some passives such as resistors and capacitors were used, but their viability for temperatures higher than 200°C was verified before being used in the actual circuit designs. No change was observed in the values of these passive components.

The current mirror and push-pull output stage were both measured using a hot chuck, while the BGR was measured using a high-temperature oven. The current mirror and push-pull output stage were measured on-wafer using special high-temperature probes, and care was taken to achieve good probe contact, which can

Table 4.1: Key temperature-dependent parameters in the Mextram compact model.

Model Parameter	Definition
AQBO	Zero bias base charge
AE	Temp. coefficient of RE
AB	Temp. coefficient for RB
AEPI	Temp. coefficient for REPI
AEX	Temp. coefficient for extrinsic RB
AC	Temp. coefficient for buried layer
DVGBF	Bandgap voltage difference of β_{F}
DVGBR	Bandgap voltage difference of β_{R}
VGB	Bandgap voltage of base
VGC	Bandgap voltage of collector
VGJ	Bandgap voltage of EB junction recombination
DVGTE	Bandgap voltage difference of emitter stored charge

be an issue at high temperatures. Given the sensitive nature of the BGR, however, it was packaged and wirebonded in a ceramic dual inline package (DIP) in order to avoid any potential probe contact issues at elevated temperatures.

4.2 Compact Model Calibration

In order to design circuits for high-temperature operation, robust, well-calibrated compact models are required. However, this is not typically possible since most calibrated models provided by foundries are usually only valid up to 125°C–150°C. There are two ways to overcome this obstacle. One is to use circuit techniques that take advantage of the predictable temperature dependence of the underlying devices to design around inferred changes at higher temperatures. While this is a valid tactic, it requires different techniques for different circuits and applications, which can complicate future designs, and is thus not desirable. The second way is to use calibrated models that are valid at these high-temperature ranges (200°C–300°C). This method is more scalable, and provides a path to more easily design a wide variety of circuits. The latter path was followed in the present work.

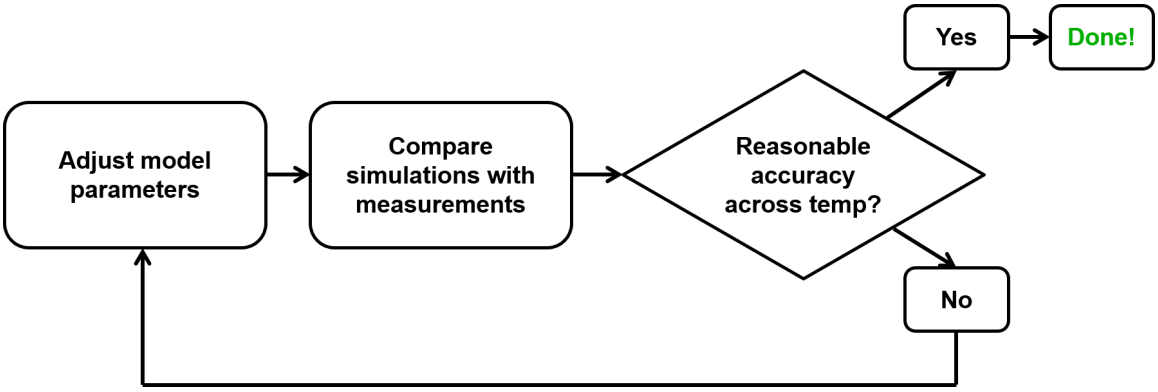


Figure 4.1: High-level diagram summary of the compact model calibration method employed in this work.

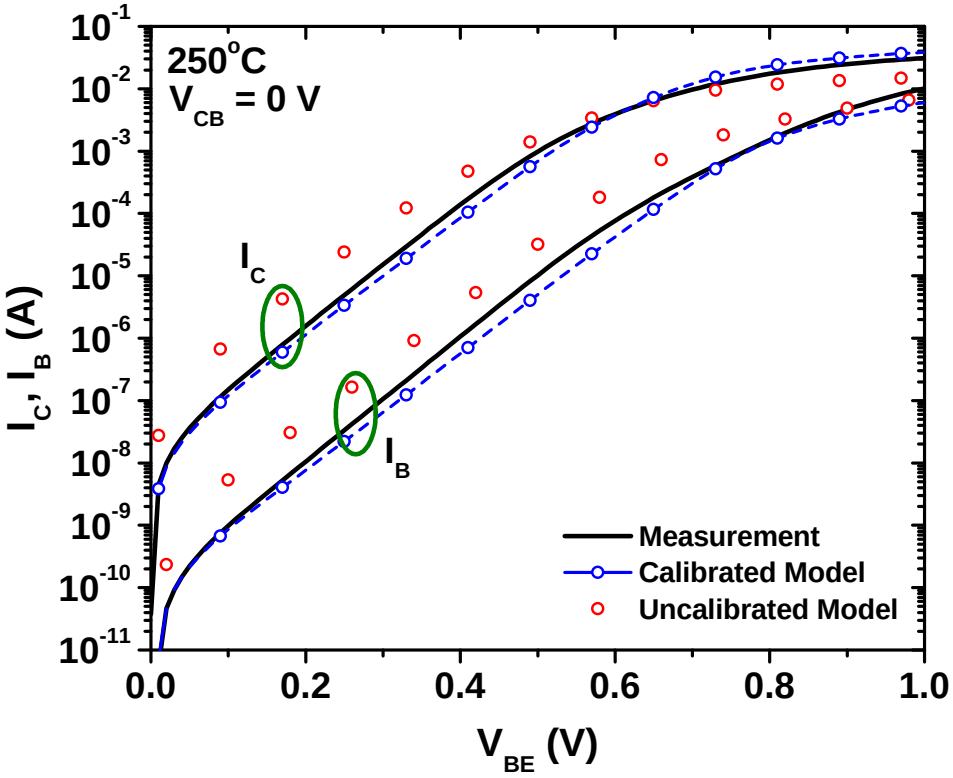


Figure 4.2: Gummel plots comparing simulation of both uncalibrated and calibrated models with measurements at 250°C.

The compact model used in this work is Mextram [83]. Temperature-dependent parameters that had a large effect on both DC and AC behavior were first identified and are listed in Table. 4.1. DC behavior of SiGe HBTs was characterized with Gummel and output family curve measurements over temperature. While a large

sample size is required to truly calibrate a compact model, that was not possible due to time and equipment constraints. A compromise was made and approximately 10 devices of four different emitter sizes were measured from 24°C–300°C, and the gathered data was then used to calibrate the compact model.

An iterative approach was taken during calibration. A high-level diagram illustrating the calibration procedure is shown in Fig. 4.1. First, Gummel and output family curves were compared with simulations, and the appropriate model parameters were tuned to ensure good calibration across a wide temperature range. A representative example of this calibration is illustrated in Fig. 4.2. Gummel simulations before and after calibration are compared with measurements at 250°C, and good agreement can be seen after calibration. It should be noted that when changing any model parameters, it is vital to ensure that no unwanted changes are made to the model behavior at other temperature ranges (i.e., the normal temperature range the compact model was previously rated for). This was confirmed with detailed simulations over several temperature ranges. Subsequently, these calibrated models were used to design high-temperature capable circuits.

4.3 Results

4.3.1 Cascode Current Mirror

A simple cascode current mirror using only NPN devices was designed (shown in Fig. 4.3) and measured from 24°C–300°C. The results are shown for 250°C in Fig. 4.4, where the output current of the mirror is plotted as a function of output voltage when the input current is varied from 5 μA–105 μA. While the results are not shown for all temperatures, these results are representative of the results over the entire temperature range of interest. Measurement results are compared with simulation results in Fig. 4.4, and there is good agreement between the two.

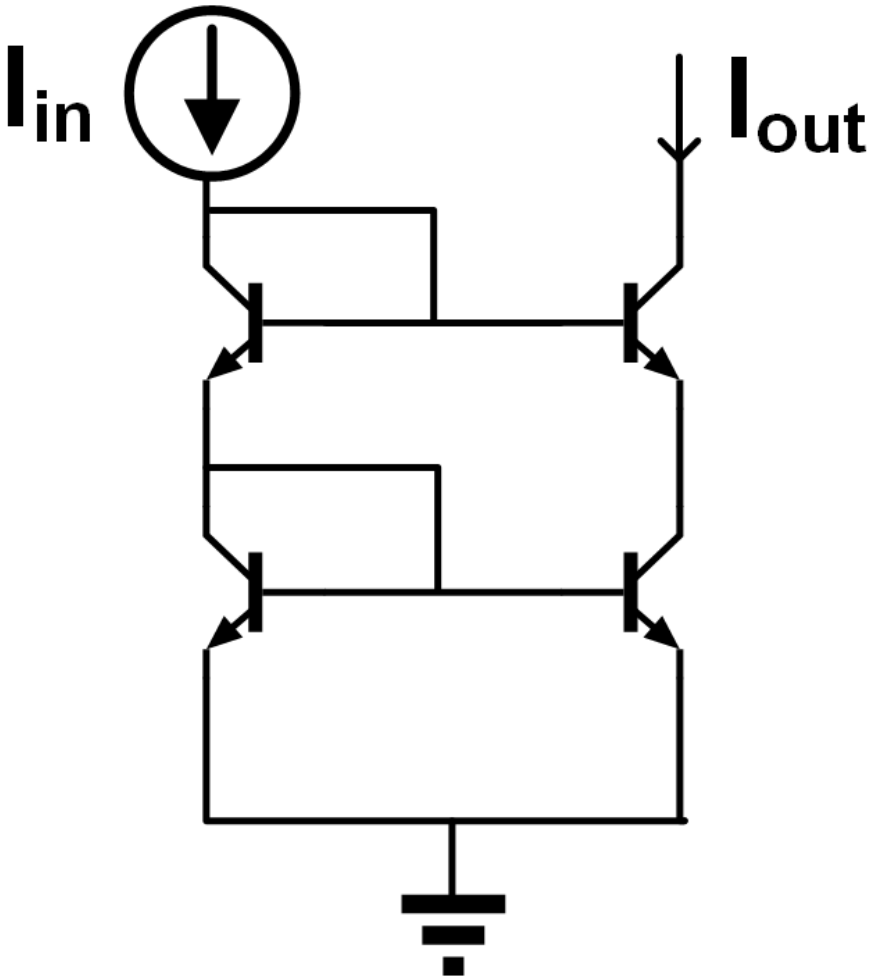


Figure 4.3: Schematic of the cascode current mirror.

Two of the key figures-of-merit (FoM) for any current mirror is its output resistance and current mirror mismatch ratio (CMMR). Both the output resistance and CMMR of the cascode current mirror were measured, and are shown in Fig. 4.5 for an input current of 105 μA. An output resistance of more than 60 MΩ was measured from 200°C–300°C. This illustrates that even though the Early voltage of SiGe HBTs decreases with increasing temperature, a cascode current mirror using SiGe HBTs still exhibits large output resistance up to 300°C, which bodes well for high-temperature operation of biasing circuits using SiGe HBTs. Another key FoM is the CMMR, which measures the percent difference between the input and output currents. A CMMR of less than 3% was measured up to 300°C. Interestingly, the CMMR gets better with

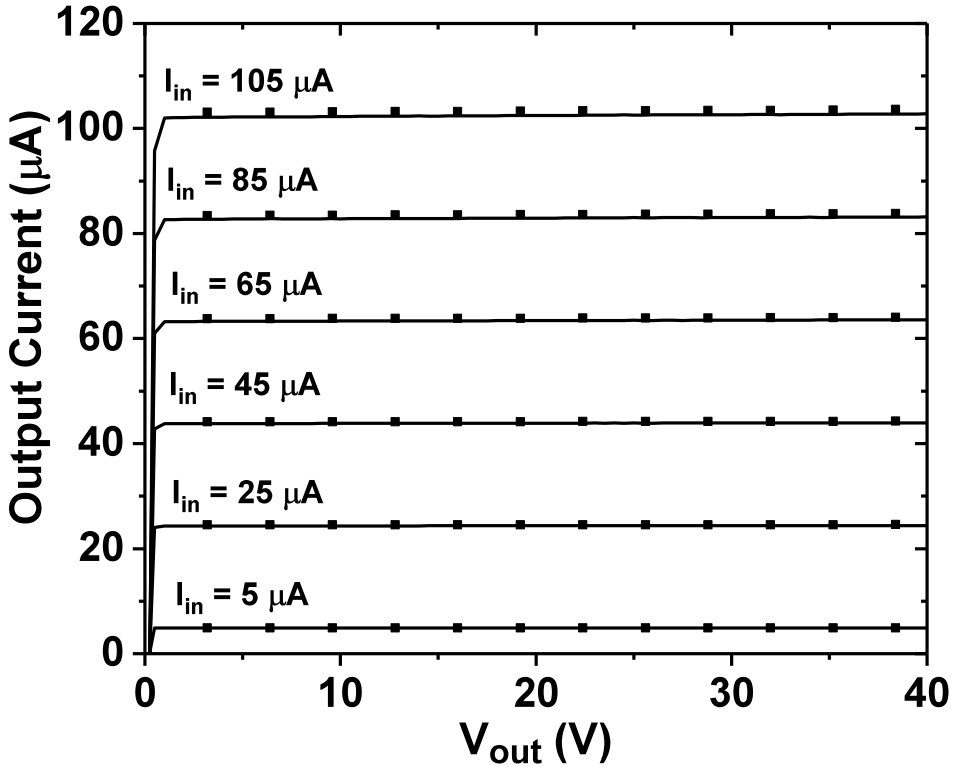


Figure 4.4: Cascode current mirror output for input current from 5 μA-105 μA as a function of output voltage at 250°C. Solid lines are measurement results and square symbols are simulation results.

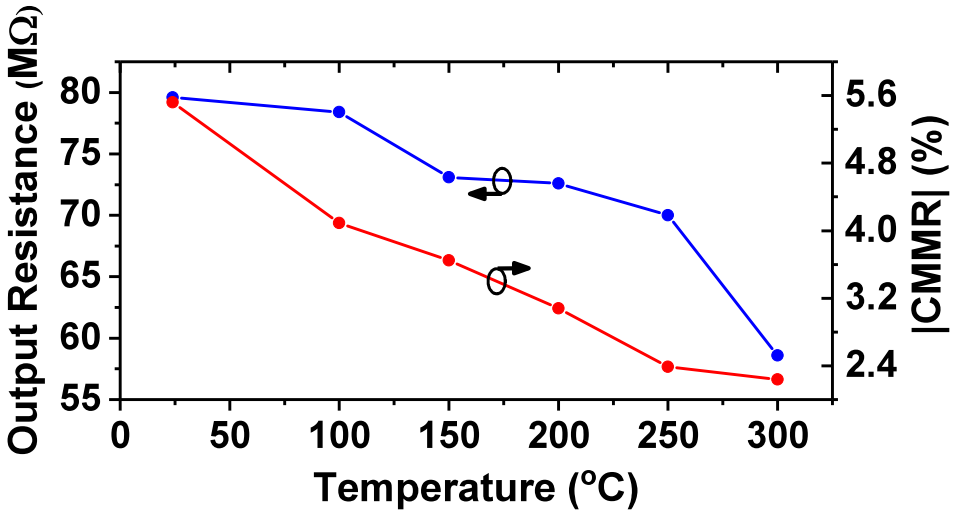


Figure 4.5: Output resistance and CMMR of the cascode current mirror from 24°C–300°C at an input current of 95 μA.

increasing temperature, which we believe is tied to the lack of temperature scaling of the current gain.

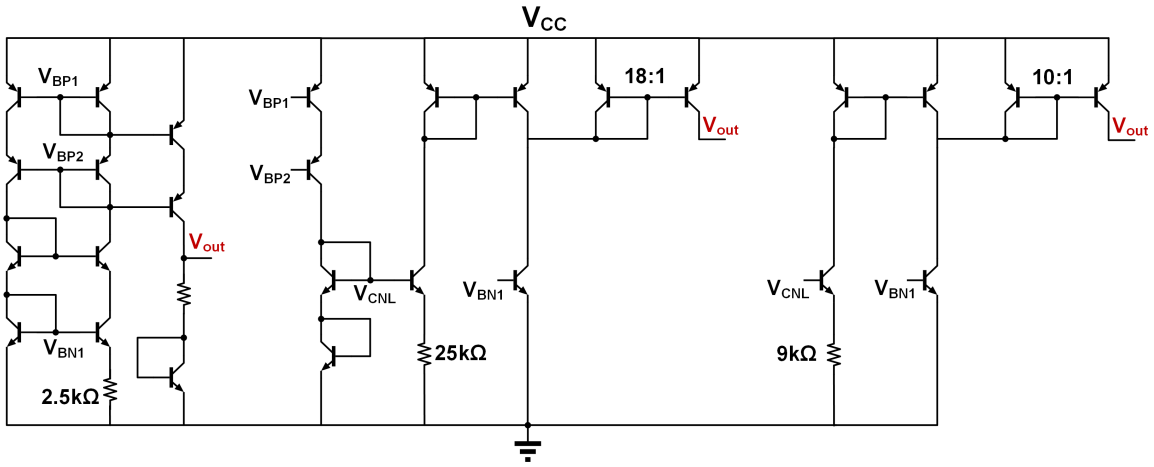


Figure 4.6: Schematic of the wide-temperature BGR.

4.3.2 Bandgap Reference Circuit

A voltage reference circuit is a ubiquitous component that provides a stable bias to other circuits across temperature. An attempt was made here to build a BGR circuit that could provide an output voltage with as small a temperature coefficient (TC) as possible from 24°C–300°C.

The design of the BGR began with a standard beta multiplier topology, as illustrated in Fig. 4.6. The standard beta multiplier by itself provides a supply-independent biasing for the core of the BGR. The core of the BGR generates a constant output voltage (V_{out}) from approximately 24°C–300°C. This is achieved by the first two branches producing a current that is proportional to absolute temperature (PTAT). This PTAT current is fed into the 25 kΩ resistor and the diode-connected transistor. The voltage drop across the 25 kΩ resistor increases with temperature, while the voltage across the diode-connected transistor decreases with increasing temperature due to the temperature dependence of V_{BE}. However, this is only true up to 125°C. Past this temperature, the complementary to absolute temperature (CTAT) voltage across the diode-connected transistor decreases faster with respect to the PTAT voltage of the 25 kΩ resistor, which results in the output voltage decreasing

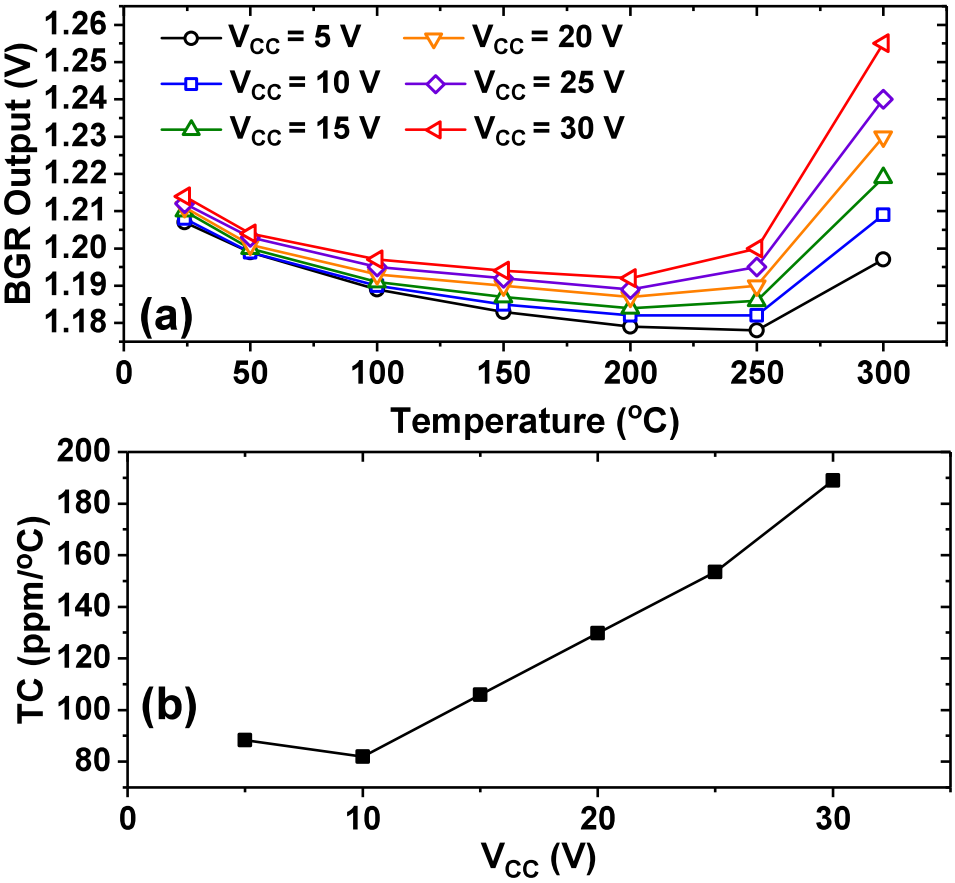


Figure 4.7: (a) Output voltage of the wide-temperature BGR from 24°C–300°C for different supply voltages (b) Measured TC of the wide-temperature BGR for different supply voltages.

after 125°C. Additional current needs to be injected into the V_{out} node with increasing temperature so that the PTAT voltage across the resistor increases proportionally with the CTAT voltage across the diode-connected transistor [84].

In order to inject additional current into V_{out} with increasing temperature, extra stages were added to the BGR, as indicated in Fig. 4.6. Each of these additional compensation stages were designed such that they are active only over their designed temperature range. Once the BGR enters this particular temperature range, these branches output extra PTAT current into V_{out}. The temperature at which these stages become active is controlled by the resistor in the stage, while the magnitude of the PTAT current injected is controlled by the current mirror ratio at the output of each stage. By properly tuning the resistor value and current mirror ratio, one can

Table 4.2: Benchmarking wide-temperature BGRs.

	This work	[82]	[85]	[86]	[87]	[88]	[89]
Technology	SiGe-on-SOI	Bulk SiGe	SOI CMOS	4H-SiC BJT	Thin-film SOI CMOS	PDSOI CMOS	GaN
V_{ref} (V)	1.201	1.187	1.18	3.16	1.2	1.167	-2.1
Temperature Range (°C)	24-300	25-225	25-250	25-500	25-300	25-300	25-250
TC (ppm/°C)	88.48	59	112	46	98	138	<238
Supply Voltage (V)	5	-	5	7.5	4	2	-9
Area (mm^2)	0.089	-	-	0.81	0.385	0.083	0.16
Power Consumption (mW)	1.7	-	1.28	29.25	0.8	0.285	7.2

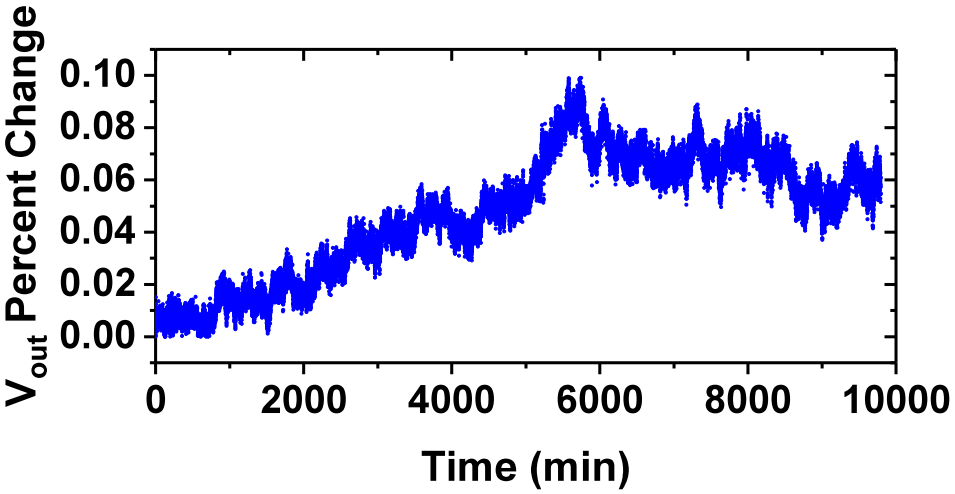


Figure 4.8: Percent change of BGR V_{out} at 300°C with a V_{CC} of 30 V as a function of time.

achieve a very low TC from 24°C–300°C. This approach has many benefits, since it allows a modular design approach. Assuming the models are well-calibrated over the temperature range of interest, this design approach enables a designer to individually control the TC over any arbitrary temperature range with multiple stages.

The measured V_{out} of this wide-temperature BGR from 24°C–300°C is shown in Fig. 4.7(a). The TC for each V_{CC} is shown in Fig. 4.7(b). A TC of 88.3 ppm/°C is

achieved at a V_{CC} of 5 V from 24°C–300°C, which to the best of the authors' knowledge, is the lowest measured TC of any silicon-based BGR over this wide-temperature range. The performance of this BGR is benchmarked with other wide-temperature BGRs found in Table.4.2. Not only does this wide-temperature BGR have the lowest measured TC in this particular temperature range, but it also compares favorably in terms of area and power consumption.

While a low TC is measured, the BGR output isn't completely ideal and has a higher TC than what was observed in simulations. Fig. 4.7 shows that the output voltage doesn't increase until past 250°C (however, the slope starts to decrease past 125°C). Ideally, the V_{out} should have several peaks and troughs, which would indicate that proper temperature compensation is occurring. This was confirmed by monitoring the total current drawn by the BGR, which ranged from 320 μA–360 μA. These values were similar to what was seen in simulations, which indicates that the different compensation stages are activating properly over their respective temperature ranges. The observed discrepancy is likely due to the injected PTAT current not increasing at a faster rate than the CTAT current. This leads to a decreasing V_{out} as observed in Fig. 4.7. This result is not surprising, since a BGR is a precision circuit and thus, any small discrepancies in the model (specifically the temperature dependence of V_{BE}) can lead to significant differences in measurements. However, this is clearly a solvable issue with better compact model calibration using a larger sample size of devices.

Long-term reliability of circuits operating at elevated temperatures is always a concern. To make sure there were no long-term reliability issues, the BGR was operated at 300°C with a V_{CC} of 30 V for approximately 10,000 minutes. The percent change in V_{out} as a function of time is shown in Fig. 4.8. Less than 0.1% change in V_{out} over 10,000 minutes was observed, and the overall effect on the TC was negligible.

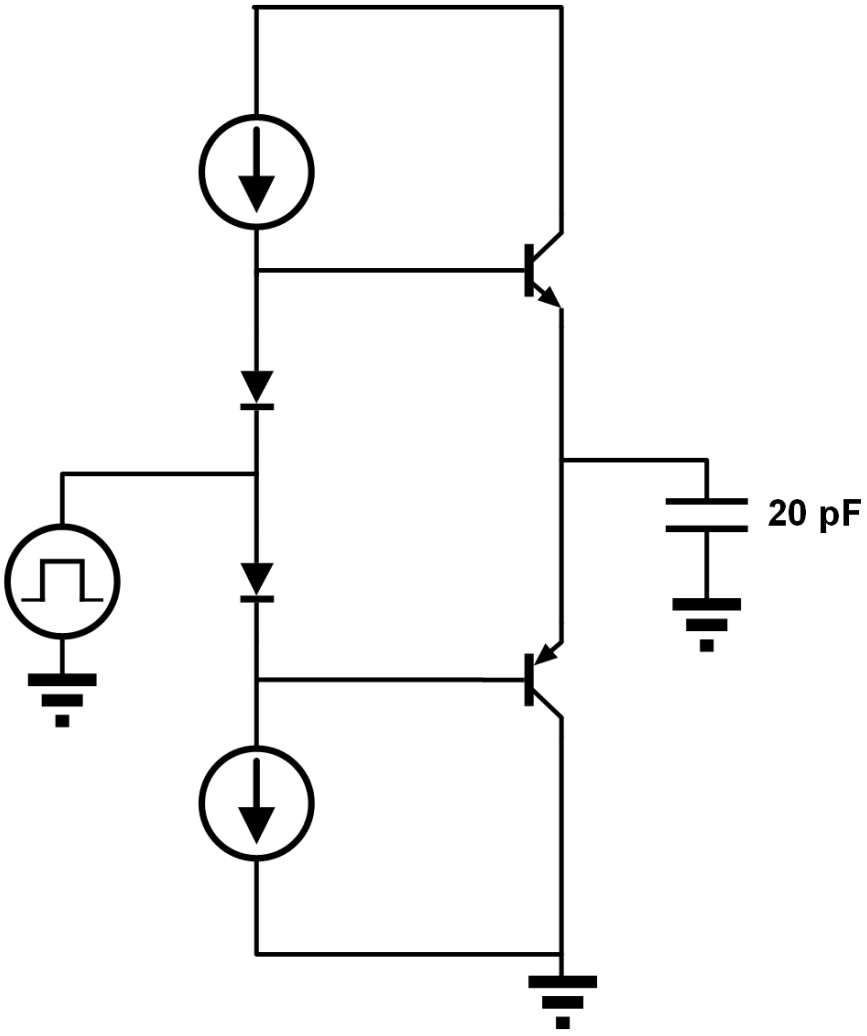


Figure 4.9: Schematic of the class AB push-pull output stage.

4.3.3 Class AB Push-Pull Output Stage

Push-pull output stages are important building blocks for most operational amplifiers since they enable an amplifier to drive large capacitive loads easily. Thus, a proper push-pull output stage that can reliably drive a given load across the entire temperature range of operation is vital for building larger analog circuits aimed at high-temperature operation. A simple class-AB push-pull output stage utilizing both NPN and PNP devices was designed for high-temperature testing and the schematic is shown in Fig. 4.9. The push-pull output stage was designed to handle up to ±20 V supply with a ±2 V input swing.

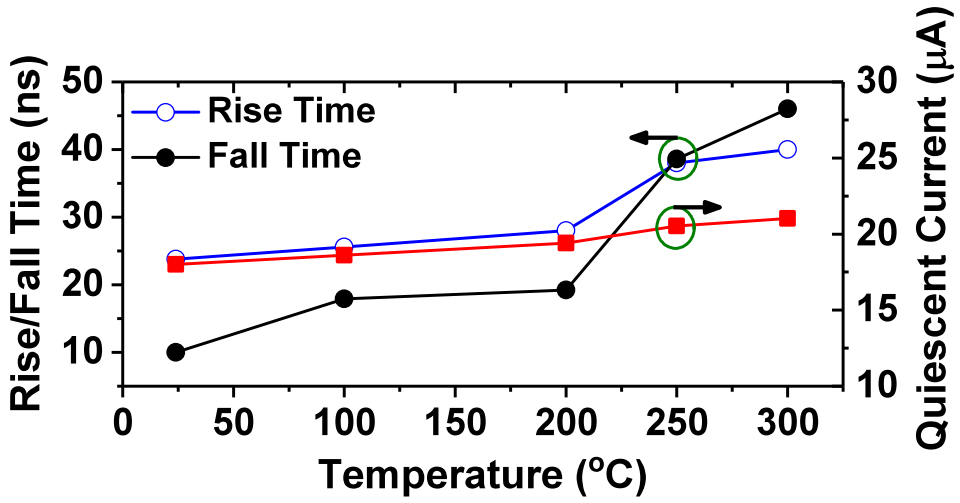


Figure 4.10: Rise and fall time of a class AB push-pull output stage driving a 20 pF load as a function of temperature. The quiescent current consumption is also shown in the right y-axis.

The push-pull output stage was tested using a 20 pF load with ±10 V supplies and a 10-kHz ±1 V square wave input signal. The rise and fall time from 24°C–300°C is shown in Fig. 4.10. In general, both the rise and fall times increase with increasing temperature. This is caused by both a reduction in transconductance (leading to a decrease in the drive current), and due to the increase in the device parasitics, specifically the junction capacitance, at high temperatures. The increase in the capacitance is mainly due to the temperature dependence of the built-in voltage (V_{bi}) [90]. An increase in the junction capacitance requires longer charging and discharging times, which contributes to the trend seen in Fig. 4.10. Interestingly, the fall time becomes slower compared to the rise time past 250°C indicating that the parasitics and transconductance associated with the PNP device change faster relative to the NPN device, since the fall time is controlled by the PNP device sinking the output current. Therefore, any circuit aimed at switching applications for high temperatures needs to account for the increase in certain device metrics at higher temperatures. While this particular design was not intended to output large current, it was still capable of sinking approximately 1 mA even at 300°C. The quiescent

current is also shown in Fig. 4.10. The benefits of using SOI is readily apparent, since there is only a small increase in the quiescent current from 24°C–300°C (18–21 μA).

4.4 Summary

SiGe-on-SOI HBTs are utilized to demonstrate the viability of using SiGe HBTs for emerging high-temperature analog applications. A method to calibrate compact models for 24°C–300°C was demonstrated. Calibrated compact models were used to build a cascode current mirror, a BGR, and a class-AB push-pull output stage. The cascode current mirror demonstrates $>$ 60 MΩ output resistance and a CMMR less than 3% at 300°C. A piece-wise linear compensation method was used to design a wide-temperature BGR and a TC of 88 ppm/°C is measured at a V_{CC} of 5 V. A simple push-pull output stage is also operational up to 300°C with a current drive up to 1 mA, and with a quiescent current less than 25 μA.

CHAPTER 5

HIGH-TEMPERATURE GATE DRIVER

High-temperature electronics are becoming more in demand due to the growing need in the energy, automotive, and aerospace sectors [13, 15, 29]. In particular, there is a strong need for power converters in all the aforementioned sectors. Power converter applications typically utilize large, high-breakdown devices like SiC FETs [91]. Their large breakdown, high switching speeds, and robustness at high temperatures make them very appealing as power switches. These power converters will typically face high temperatures with under-the-hood automotive components reaching 150-250°C, deep oil-well digging reaching temperatures as high as 300°C, and geothermal reaching even higher temperatures [13].

These large SiC FETs in power converter applications require a gate driver and other control circuitry to effectively switch. The effective capacitance of these SiC FETs easily exceed 1 nF, and therefore, large source and sink currents are required to switch these FETs rapidly to minimize switching loss. Additionally, the gate driver in particular needs to be as close as possible to the SiC FETs in order to reduce parasitics, which has a large impact on the peak drive current. Consequentially, the gate driver has to be capable of operating reliably at elevated temperatures.

As shown in the previous chapters, SiGe-on-SOI HBTs have shown adequate performance and reliability even at temperatures as high as 300°C. High-performing circuits were also shown to be viable with the analog building blocks that were discussed in Chapter 4. This chapter aims to take it a step further and explore the design and performance of a gate driver circuit using SiGe-on-SOI. High-temperature

gate drivers operational up to 225°C using SOI CMOS have been demonstrated previously [91,92]. However, very little work has been reported for gate driver operation up to 300°C, which can be encountered in several high-temperature applications. This work presents a high-temperature (up to 300°C) capable gate driver built using SiGe-on-SOI HBTs with multi-amp drive capabilities.

5.1 Technology and Measurement Details

A 48-V C-SiGe-on-SOI HBT platform is used in this work [77]. The devices were optimized for high-breakdown voltage, and thus have lower unity gain frequency (f_T). Therefore, these devices are better suited for analog applications. Both NPN and PNP devices were used for the design of the driver and their performance and reliability were characterized up to 300°C in previous works [3].

In order to make high-temperature measurements, a 300°C hot chuck was used for the purposes of this work. All measurements were made on-wafer using high-temperature capable probes. GGB probes were used for both AC and DC signals, while a Cascade Microtech high-current (6-A pulsed current) probe was used for the supply voltage. A 100 MHz, Tektronix function generator was used as a pulse-width modulator (PWM) source, and a 100 MHz oscilloscope was used to measure the output signal. Keithley source-measure units (SMUs) were used for the DC biasing.

5.2 Driver Design

Similar to the work in [4] and the previous chapter, a calibrated compact model for both NPN and PNP devices across temperature was obtained. Using the calibrated compact models, a high-temperature capable driver was designed. The core function of the driver was to take an input 0-5 V square wave and switch a large power FET (e.g SiC FET) quickly with a rail-to-rail voltage output. To achieve this, a two-stage, simple driver was implemented. A high-level schematic of the driver is shown in Fig. 5.1. The input stage of the driver consists of a standard operational

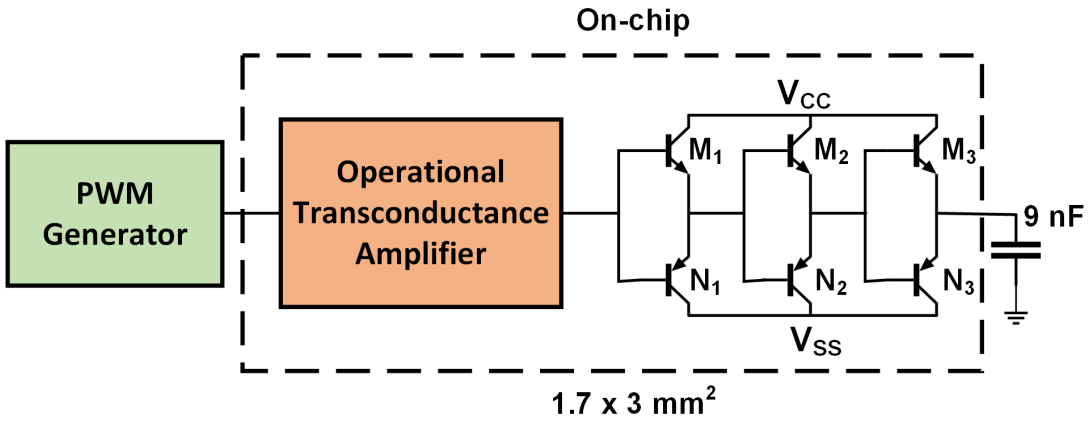


Figure 5.1: High-level schematic of the high-temperature driver.

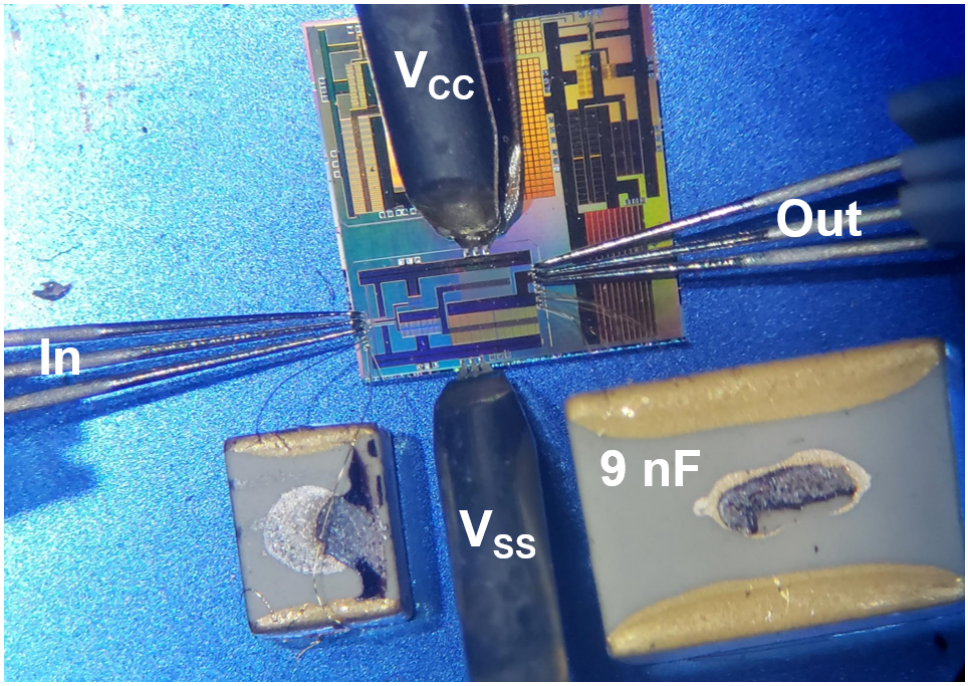


Figure 5.2: High-temperature gate driver measurement setup.

transconductance amplifier (OTA), which converts the 0-5 V square-wave signal into a rail-to-rail signal. The OTA was designed to handle signals with frequency ranging from 1 kHz - 1 MHz.

The output stage of the driver consists of a cascaded push-pull configuration. The largest available devices in the technology ($>$ 150 μm L_E) were used to achieve the maximum current drive. A three-stage cascaded push-pull amplifier was implemented

with each successive stage having larger total effective area. The M:N ratio between the NPN and PNP devices in the push-pull configuration was carefully optimized to get similar source and sink current. Gummel measurements along with output characteristics were performed on these devices across temperature, and the results indicated that the NPN devices were capable of sourcing up to 2.5X more peak current than the PNP devices. Additionally, this difference in peak current was found to be slightly temperature dependent. In order to correct for this discrepancy, the M:N ratio was appropriately skewed to get a symmetric current drive from 200°C - 300°C. This particular temperature range was more emphasized for the design since the driver was primarily intended to show operation at high temperatures.

Self-heating is also a concern when operating these devices at high currents. In order to minimize the impact of self-heating, the number of devices at each stage was carefully optimized. In doing so, the maximum current each device carries at any given temperature was properly controlled to ensure thermal runaway does not occur. This maximum current was found with the measurements detailed in [3], which found the critical collector current density at which thermal runaway was observed. Mutual self-heating is another concern with multiple devices in parallel carrying high currents. This was addressed in layout by performing a careful trade-off between total chip area and maximum reliability. Device-to-device spacing of 1-2 μm was used to reduce mutual self-heating as much as possible to prevent any current crowding effects. Electromigration is another key concern associated with high-temperature operation. In order to mitigate potential electromigration issues, extremely wide metal lines ($>$ 150 μm) along with several thousands of redundant vias were used to minimize the current density along the metal lines and vias.

While the driver was meant to switch a large power FET, a large capacitor was instead used for testing purposes. Since the large power FET is essentially a large capacitor that is meant to be charged and discharged rapidly, the use of a capacitor

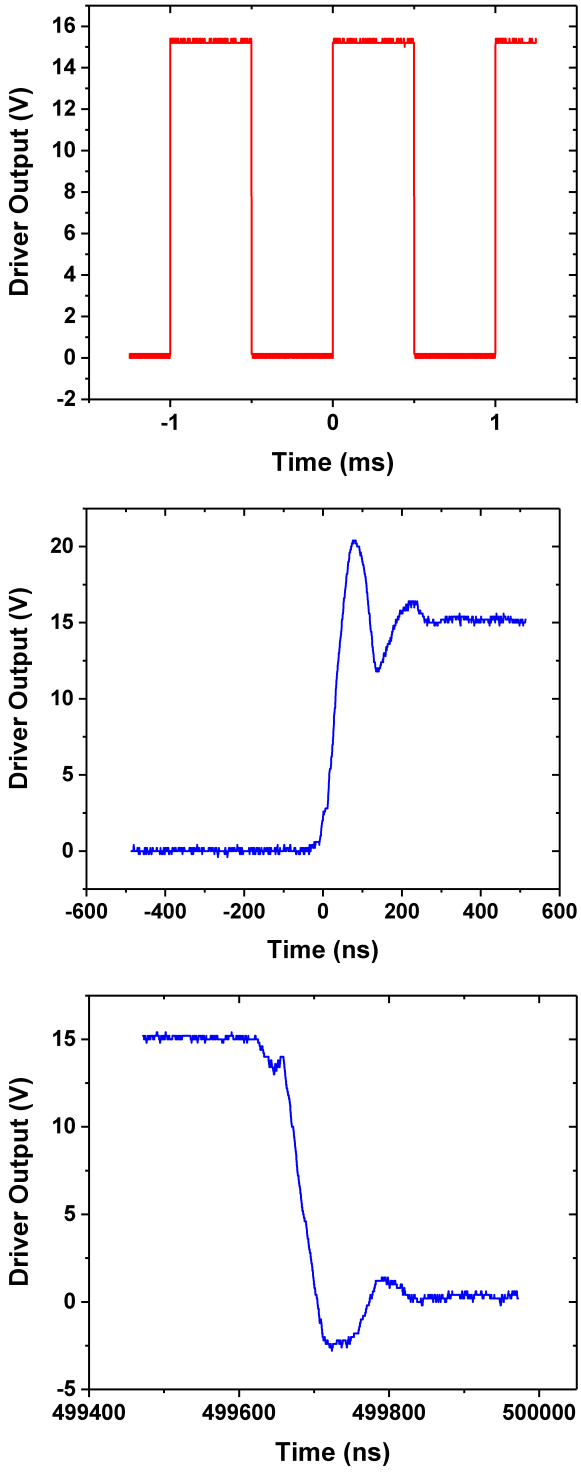


Figure 5.3: Output voltage of the gate driver measured at 250°C with a 0-5 V, 1 kHz square wave input. Rise and fall time of 48 ns and 40 ns were measured with a 9 nF capacitor, respectively.

for simulation and testing was deemed appropriate. The total area of the driver was measured to be 1.7 x 3 mm^2. A large portion of this area was due to the output stage.

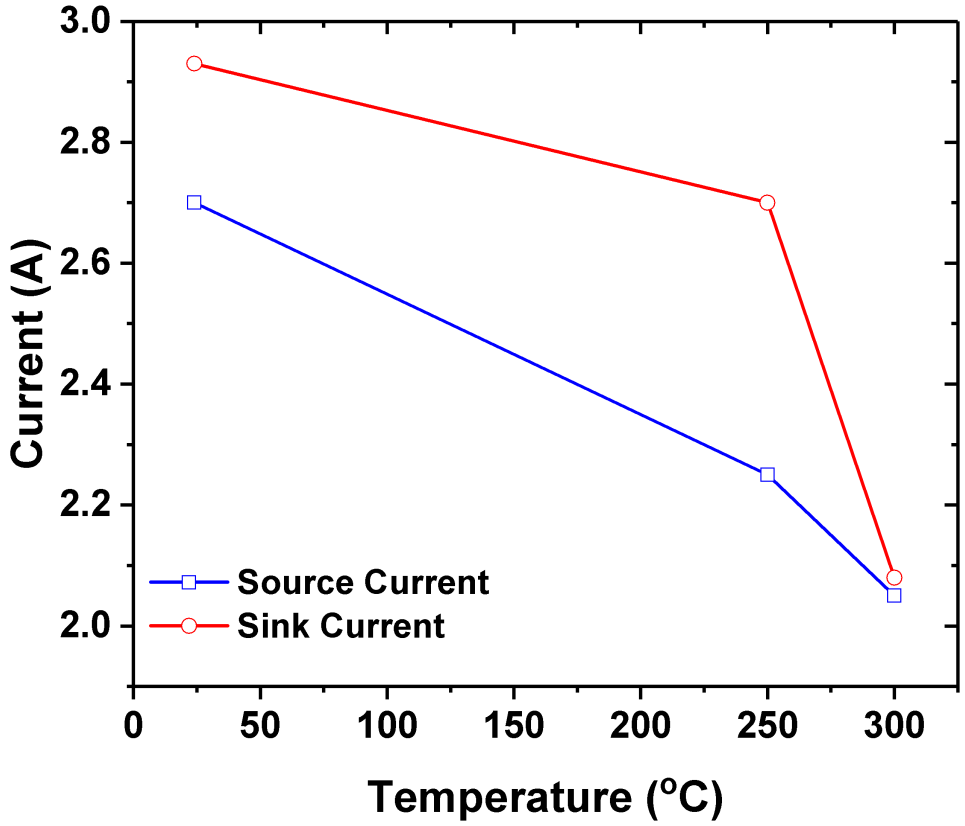


Figure 5.4: Peak source and sink current of the driver across temperature from 24°C - 300°C.

5.3 Results and Discussion

In order to perform on-wafer probing, the driver die along with external wirebondable capacitors were affixed to an underlying plain silicon substrate. Wirebonds were then made from the output pads to the capacitor. To reduce inductance and resistance at the driver output, the capacitor was placed as close as possible to the driver die and up to three parallel wirebonds were made. Both the epoxy used to affix the die and capacitor along with the wirebonds were all verified operational up to 300°C. The capacitors used in this work were special, custom capacitors specifically meant for up to 300°C operation. A picture of the setup along with the die and the probes are shown in Fig. 5.2.

A 0-5 V, 1 kHz square wave was applied to the input of the driver, and the output

voltage waveform was captured by the oscilloscope. The results at 250°C are shown in Fig. 5.3. A V_{CC} of 15 V and a V_{SS} of 0 V was used. The output of the driver is able to reach both rails within ±100 mV across all the measured temperature conditions.

The peak current drive of the driver was measured by analyzing the rising and falling edge of the output voltage waveform as shown in Fig. 5.3. At 250°C, a rise and fall time of 48 ns and 40 ns were measured, respectively. The peak currents were then calculated based on these rise and fall times. The source and sink currents were calculated to be approximately 2.32 A and 2.73 A, respectively. To the best of the author's knowledge, these are the highest measured source and sink currents for a driver at 250°C using a silicon-based technology. Overshoot and some ringing is observed in the output waveform. Simulations were performed by adding up to 1-10 nH of inductance to the output path, and a similar type of ringing was reproduced. It is likely that parasitics both from the wirebond and probes are contributing to this behavior.

The peak current drive was also measured across temperature and it is shown in Fig. 5.4. Up to 28% reduction in the sink current and 23% reduction in the source current is observed as temperature increases from 24°C - 300°C. A similar reduction in peak current drive with increasing temperature for a simple push-pull output stage was demonstrated in [4]. This is mainly attributed to a reduction in transconductance with increasing temperature along with higher device parasitics (mainly capacitance) leading to an overall decrease in the peak current drive. It is also possible that small increases in the output resistance due to a change in the metal resistance at high temperature could play a role in decreasing the peak current drive.

While a comprehensive reliability test could not be performed, the driver was left operating with a V_{CC} of 25 V at 300°C for up to 6 hours, and no observable change in the driver performance was seen. Long-term testing (> 10,000 minutes) will need to be performed to rule out any potential electromigration or high-current induced

stress failure.

5.4 Summary

This work demonstrates an operational, high-temperature gate driver using a C-SiGe-on-SOI technology. A calibrated compact model was constructed, and the compact model was subsequently used to design a driver circuit that could switch a 9 nF load in under 50 ns. A simple circuit architecture was used with an operational transconductance amplifier with a cascaded push-pull output stage implemented. Proper ratio of NPN and PNP devices was used to account for differences in their current drive. Based on previous reliability studies, appropriate steps were taken to make sure peak current carried by a single device does not lead to reliability issues. The fabricated driver was tested on-wafer with an external 9 nF capacitor at temperatures high as 300°C using a hot chuck. At 250°C, peak source and sink current of 2.32 A and 2.73 A were measured, respectively. A reduction in current drive is observed with increasing temperature due to a decrease in transconductance and an increase in device parasitics.

CHAPTER 6

TOTAL IONIZING DOSE EFFECTS IN A HIGH-VOLTAGE SIGE HBT TECHNOLOGY

The investigation of total ionizing dose (TID) effects on a high-voltage (36 V) complementary thick-film SOI SiGe technology is investigated for the first time. SiGe platforms provide high-speed heterojunction bipolar transistors (HBTs) that enable performance-constrained RF applications such as LNAs, PAs, mixers, oscillators, etc. However, there is also a large and growing interest in using SiGe HBTs in the analog domain. While Ge incorporation and grading in the base of a SiGe HBT significantly reduces the carrier transit time, it also enhances the current gain (β) and the Early Voltage (V_A), and both device parameters are important metrics for analog applications.

Many investigations have been performed on the TID tolerance of SiGe HBTs from 1st generation to 4th generation devices [39,56,93,94]. These studies have consistently shown that SiGe HBTs are multi-Mrad tolerant, primarily due to their structure, not the Ge, per se. Recent work has also been done on a thick-film complementary SOI 5 V SiGe process that illustrated favorable TID response from both a forward-mode and inverse-mode operation [95]. However, the TID response of a high-voltage ($>$ 30V) complementary SOI SiGe HBT has never been investigated. As high-voltage-capable devices utilize lower doping to reduce peak electric fields at larger voltages, they also tend to have larger depletion regions near oxide interfaces that could potentially adversely impact its TID response. The chapter investigates the TID response of a 36 V complementary thick-film SiGe HBT on SOI and its potential for use in high-voltage radiation applications.

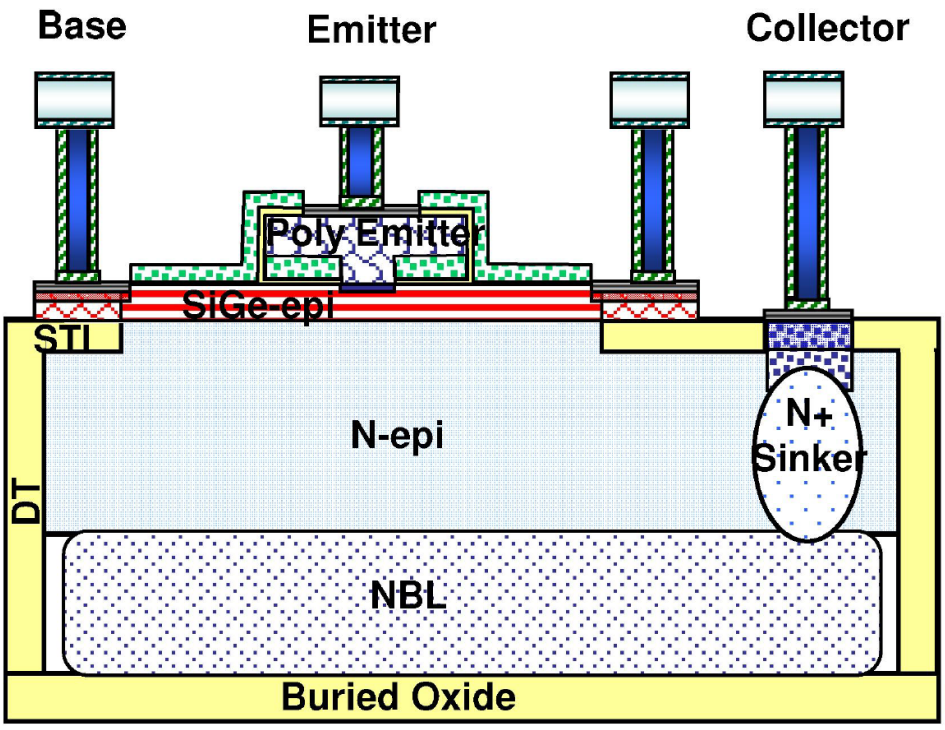


Figure 6.1: A cross-section of the 3HV NPN [77].

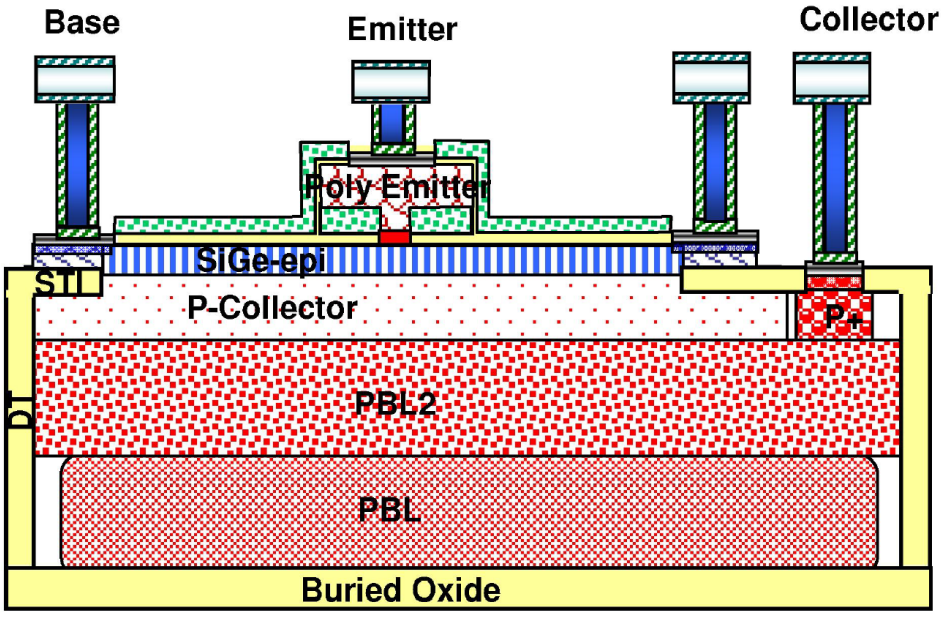


Figure 6.2: A cross-section of the 3HV PNP [77].

Table 6.1: Table summarizing the values of key performance metrics for the NPN and PNP used in this work [77].

Parameter	NPN	PNP
β	200	230
V_A	<-100	>100
BV_{CEO}	48	-53
BV_{CBO}	53	-53
Peak f_T ($12V_{CB}$)	4.2 GHz	3.0 GHz

6.1 Experimental Details

A device cross section of the 3HV NPN and PNP used in this work is illustrated in Fig. 6.1 and Fig. 6.2, respectively. The NPN and PNP devices are SOI devices, built on top of a 0.4 μm thick buried oxide (BOX). The devices were optimized for a high β-V_A product while maintaining a BV_{CEO} up to 48 V [77]. Key device metrics are summarized in Table 6.1. As these devices are optimized for high-voltage analog applications, it does utilize a thicker collector epi with lower doping than what is typically found in modern SiGe HBTs that are aimed more towards high-speed (e.g., RF) applications. The TID experiments were performed at Vanderbilt University and the Naval Research Laboratory (NRL) using a 10-keV X-ray ARACOR test system. The devices were wirebonded out in a 28-pin dual-in-line package (DIP) and then irradiated from 50 krad(SiO_2) to a cumulative dose up to 5 Mrad(SiO_2), at a dose rate of 32.5 krad(SiO_2)/min. All devices used in the present work were 0.4 μm emitter-width devices.

Pre-irradiation *dc* characteristics were measured and then after each subsequent dose, the *dc* characteristics were once again remeasured to track the change in response with increasing total dose exposure. Gummel characteristics were primarily used to characterize the *dc* behavior. Three different bias conditions were investigated. The first condition was with all the terminals grounded, as it is considered the worst-case condition for bipolar devices in general [96]. The second condition was

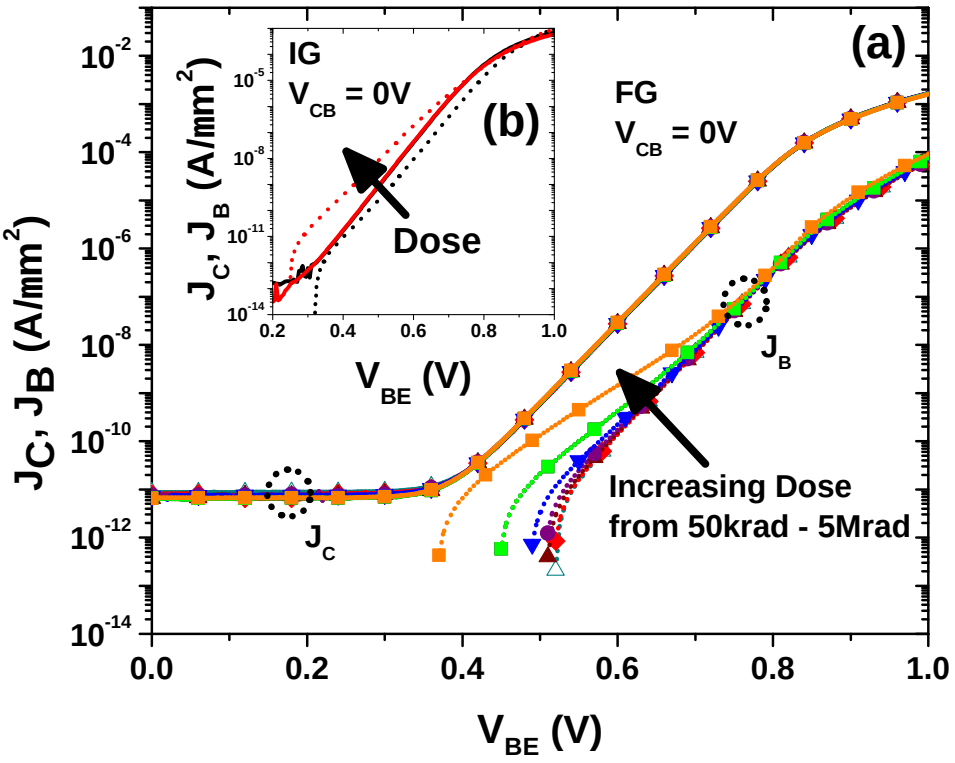


Figure 6.3: (a) Forward Gummel of the NPN (grounded condition) for the following cumulative doses: pre-rad, 50 krad(SiO_2), 100 krad(SiO_2), 300 krad(SiO_2), 500 krad(SiO_2), 1 Mrad(SiO_2), 2 Mrad(SiO_2), and 5 Mrad(SiO_2). (b) Inverse Gummel of the NPN for pre-rad and 5 Mrad(SiO_2). Solid lines are J_C and dotted lines are J_B.

with a V_{BE} of 0.6 V and a V_{CB} of 10 V (referred to as "Bias 1" in this work). The third condition is with a V_{BE} of 0.6 V and a V_{CB} of 20 V (referred to as "Bias 2" in this work). The second and third conditions were chosen to determine whether high-voltage operation can potentially influence the TID response. It should be emphasized that the bias conditions used in this work are not high enough to cause mixed-mode electrical stress damage and thus all results presented here were not influenced by impact ionization triggered damage. All bias conditions were realized using Keithley SMUs. The devices were measured in both forward-active and inverse-mode to better understand their disparities in damage mechanisms at the emitter-base (EB) spacer oxide, the STI, and the underlying buried oxide (BOX). Forward-active is typical for SiGe HBT device operation with the base-emitter junction forward-biased and the

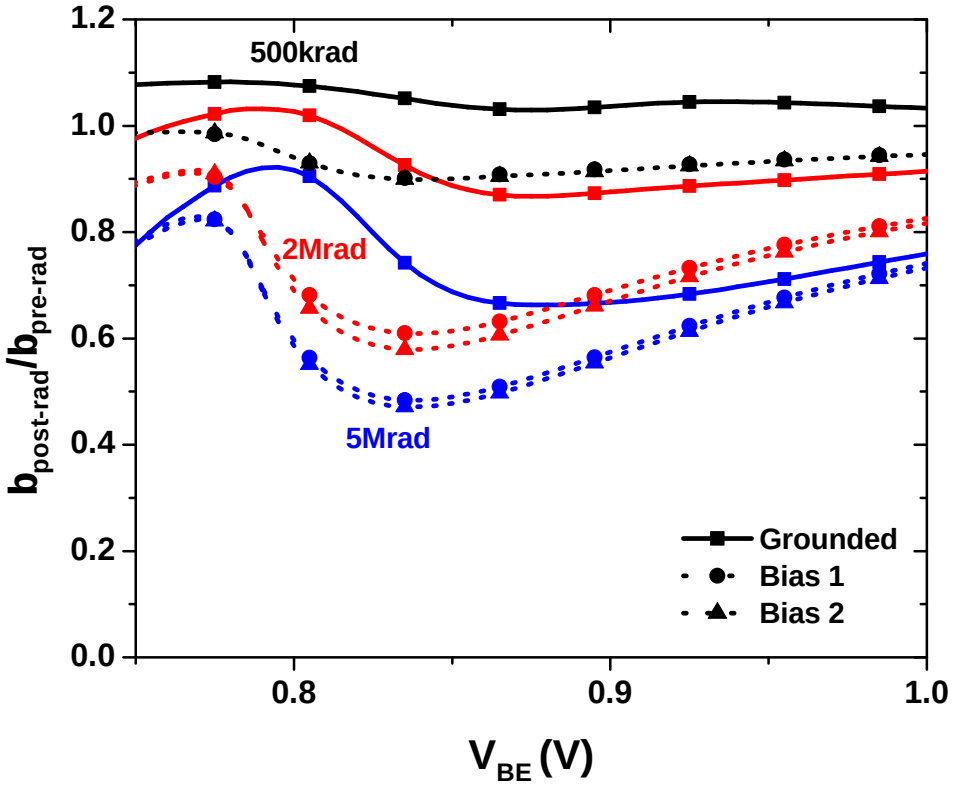


Figure 6.4: Normalized current gain (grounded condition, Bias 1, and Bias 2) post- and pre-radiation for the NPN as a function of V_{BE} for the following cumulative doses: 500 krad(SiO_2), 2 Mrad(SiO_2), and 5 Mrad(SiO_2). Solid lines are grounded condition while dotted lines correspond to Bias 1 and Bias 2.

base-collector junction reverse-biased. Inverse-mode operation swaps the electrical emitter and collector, with the physical base-collector junction forward-biased and the base-emitter junction reverse-biased (i.e. device is operated "upside-down").

6.2 TID Results

The grounded condition for the NPN was initially measured and the Gummel response is illustrated in Fig. 6.3. Fig. 6.3(a) shows the forward Gummel (FG) response, and it can be seen that there is an increase in base current density (J_B) at low and medium injection with increasing dose, as expected. The inset plot, Fig. 6.3(b), illustrates the inverse Gummel (IG) response at pre-rad and 5 Mrad(SiO_2), which shows a similar response as the FG in Fig. 6.3. No major shift ($< 5\%$) in the collector current in

both forward-mode and inverse-mode is observed, indicating that there is not enough lateral charge accumulation under the EB spacer oxide to significantly affect the total emitter area [44].

The normalized change in β as a function of V_{BE} for three different doses is illustrated in Fig. 6.4, for all three bias conditions. The low to mid V_{BE} shift in β is expected, while surprisingly, there is a significant shift at high injection (> 0.8V) which shows a very strong bias dependence. At a dose of 500 krad(SiO_2), the grounded condition shows little degradation; however, both Bias 1 and Bias 2 conditions show significantly higher degradation up to a 10% reduction in peak current gain in this V_{BE} region. At the larger doses of 2 Mrad(SiO_2) and 5 Mrad(SiO_2), the difference is even more emphasized. It should also be noted that while the difference is small, there is a clear difference (2-4%) between Bias 1 and Bias 2 at the larger doses, which illustrates that increasing V_{CB} does in fact worsen this current gain reduction.

To better understand this phenomenon, the excess J_C and J_B were examined at different doses. While J_C showed minimal change for the grounded condition, this was not entirely the case for Bias 1 and Bias 2 (>5%). However, this large change was only observed at very large doses (>2 Mrad(SiO_2)). Regardless, J_B was the primary cause in the β reduction, even at high injection, as illustrated in Fig. 6.5. While J_C, and consequently J_E, did show some change, it is clear that there is not a significant change in emitter resistance, since emitter resistance degradation results in a downward shift of both collector and base current, which is not observed here. Consequently, this implies that a different mechanism is causing a shift at high injection. J_B shift at high injection has been observed before in [97] with high-current electrical stress, which can lead to trap states at the interfacial oxide between poly/monosilicon regions. TCAD simulations investigating this phenomenon are presented in the next section.

The excess normalized difference in I_B at a V_{BE} of 0.6 V for the forward- and inverse-mode is illustrated in Fig. 6.6 for the grounded condition, along with some

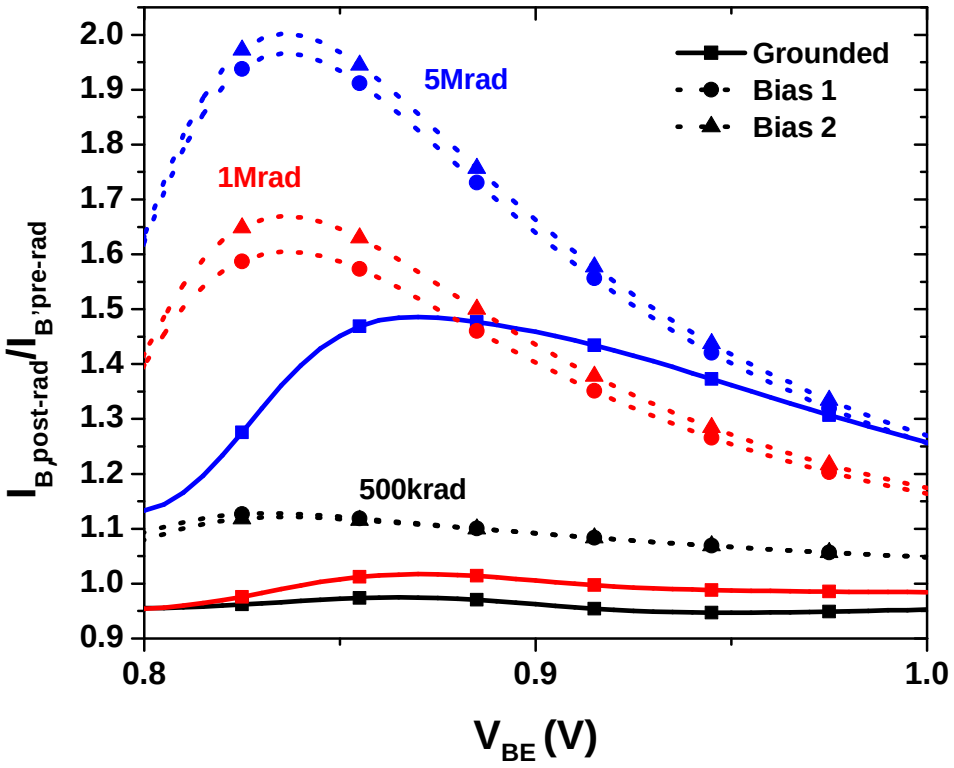


Figure 6.5: Normalized I_B (grounded condition, Bias 1, and Bias 2) post- and pre-radiation for the NPN as a function of V_{BE} for the following doses: 500 krad(SiO_2), 1 Mrad(SiO_2), and 5 Mrad(SiO_2). Solid lines are grounded condition while dotted lines correspond to Bias 1 and Bias 2. Only the high-injection bias is shown.

other SiGe technologies for comparison. It can be clearly seen that inverse-mode displays greater than 2X increase in I_B relative to the forward-mode at high doses ($>$ 1 Mrad(SiO_2)). This is attributed to the larger surface area of the STI oxide relative to the EB spacer oxide, which leads to more interface traps and oxide charge concentration [95]. Additionally, due to the lower collector doping, the larger depletion region adjacent to the STI oxide also contributes to a large surface area exposed for SRH recombination. In addition, it is worth noting that for a more aggressively scaled (130nm) SiGe technology, forward-mode damage is much higher than inverse-mode damage.

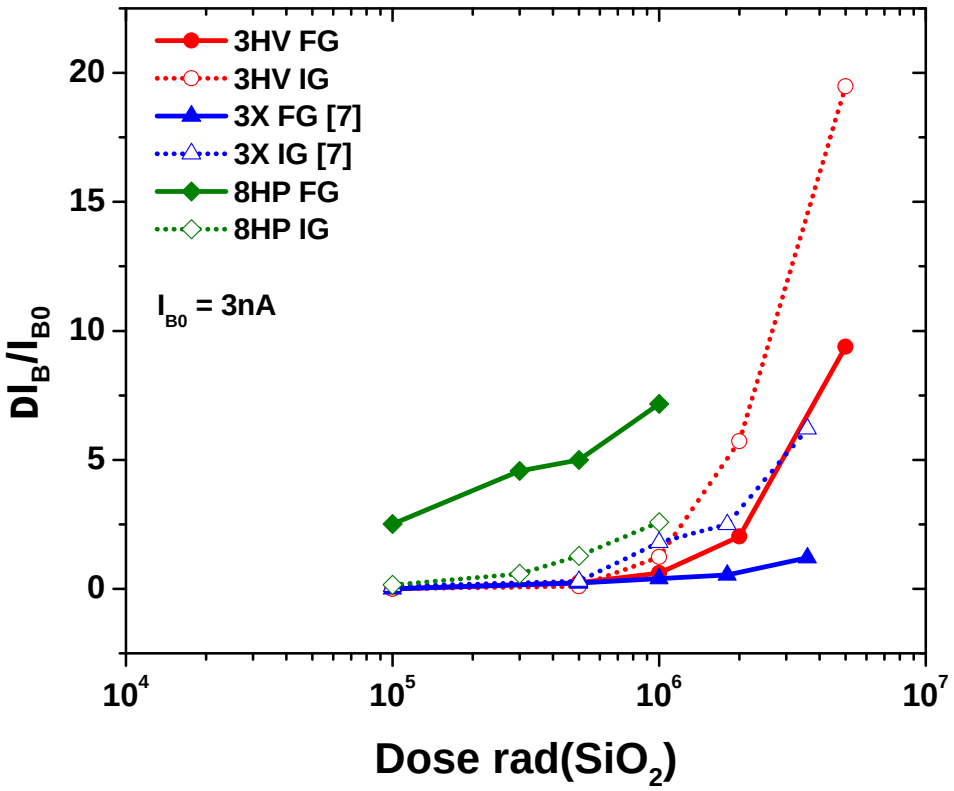


Figure 6.6: Excess normalized I_B for the NPN as a function of dose. The 3X and 8HP SiGe technology are compared with the results for the 3HV platform for both forward and inverse-mode.

As the high-injection gain reduction showed a clear bias dependence, the low-injection change was analyzed as a function of bias in Fig. 6.7. Forward-mode operation shows minimal bias dependence, which is consistent with previous TID studies; however, in the inverse-mode operation, there is a significant difference under the two different bias conditions. Specifically, there is up to a 35X difference between the grounded and two high-voltage bias conditions, an effect which has not been previously reported. This difference can be explained by looking at the electric field differences in the device between the two bias conditions. Calibrated TCAD simulations were performed at the three bias conditions, and it was seen that the electric field near the STI had far higher peaks (2-3 orders of magnitude) under HV bias. The larger electric field near and within the STI region under the HV-bias condition results in more of the electrons being swept away from the STI during irradiation,

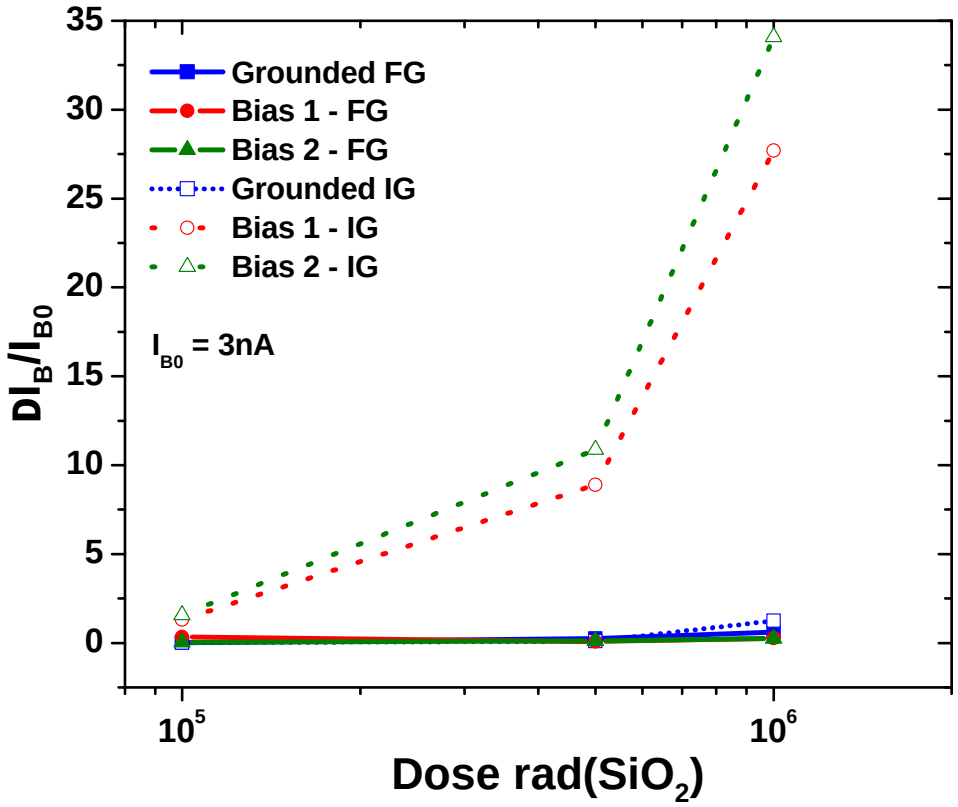


Figure 6.7: Excess normalized I_B for the NPN as a function of dose for forward and inverse-mode grounded and other bias conditions.

leaving more holes in the oxide and resulting in the higher leakage current [95]. This result is important, as it couples the high-injection effect observed in Fig. 6.4 to the physical location that helps manifest the reduction in high-injection current gain. In other words, as there is a clear and significant increase in inverse-mode leakage current with increasing V_{CB}, it becomes clear that the charge/interface traps at this interface are potentially driving the observed high-injection effect.

Similar to the NPN, the PNP SiGe HBT was also first irradiated under grounded conditions. The results are shown in Fig. 6.8. Fig. 6.8(a) shows the forward Gummel response from 50 krad(SiO_2) to 5 Mrad(SiO_2) while Fig. 6.8(b) shows the inverse-mode Gummel response. Both responses are qualitatively similar to the NPN data. However, at least for the grounded condition, the PNP shows significantly lower J_B leakage current in both forward- and inverse-mode at large doses. This difference is

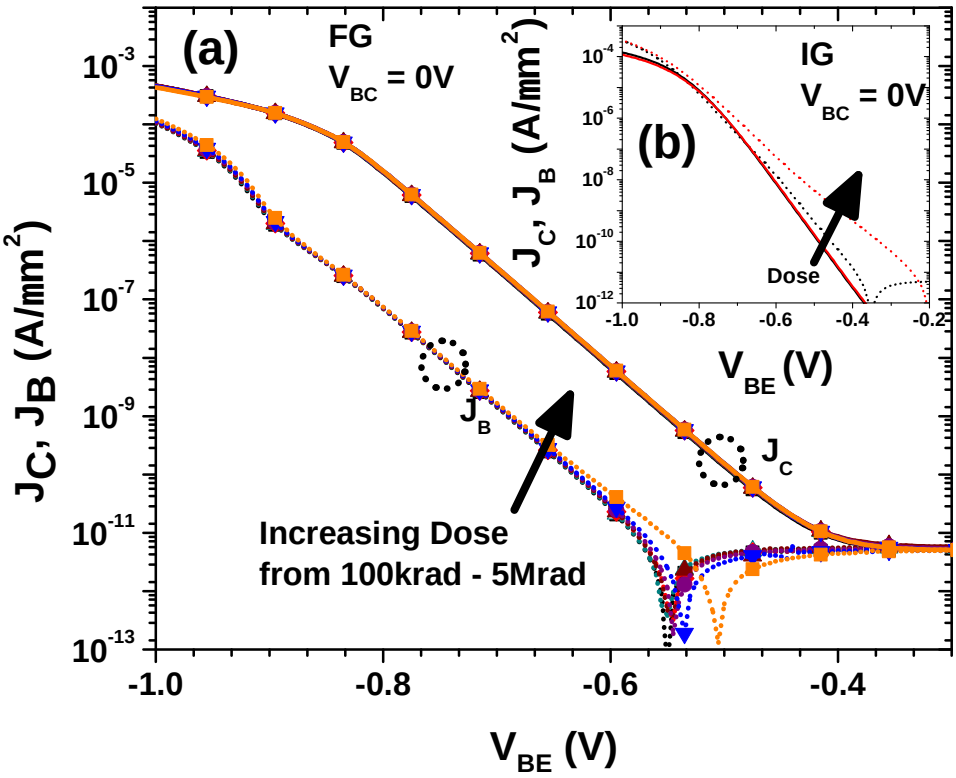


Figure 6.8: (a) Forward Gummel of the PNP (grounded condition) for the following cumulative doses: pre-rad, 100 krad(SiO_2), 300 krad(SiO_2), 500 krad(SiO_2), 1 Mrad(SiO_2), 2 Mrad(SiO_2), and 5 Mrad(SiO_2). (b) Inverse Gummel of the PNP for pre-rad and 5 Mrad(SiO_2). Solid lines are J_C and dotted lines are J_B.

more clearly illustrated in Fig. 6.9. Only 1-2X increase in forward-mode I_B and 1.2-4X increase in inverse-mode I_B is observed in the PNP. This leakage is 5-7X lower than the leakage current observed in the NPN under the same conditions. We believe that this is due to the accumulation of positive charge in the PNP oxides near the n-type base, which helps to increase the electron concentration and reduce the excess I_B due to surface recombination [98]. In Fig. 6.9, the forward and inverse-mode response is also compared with the complementary 5 V technology presented in [95], and it shows that the forward-mode response is comparable, while the inverse-mode change is much higher. This discrepancy is likely due to a larger depletion region at the collector-base junction resulting from the lower doping, which in turn leads to a larger surface area available on the STI-silicon interface.

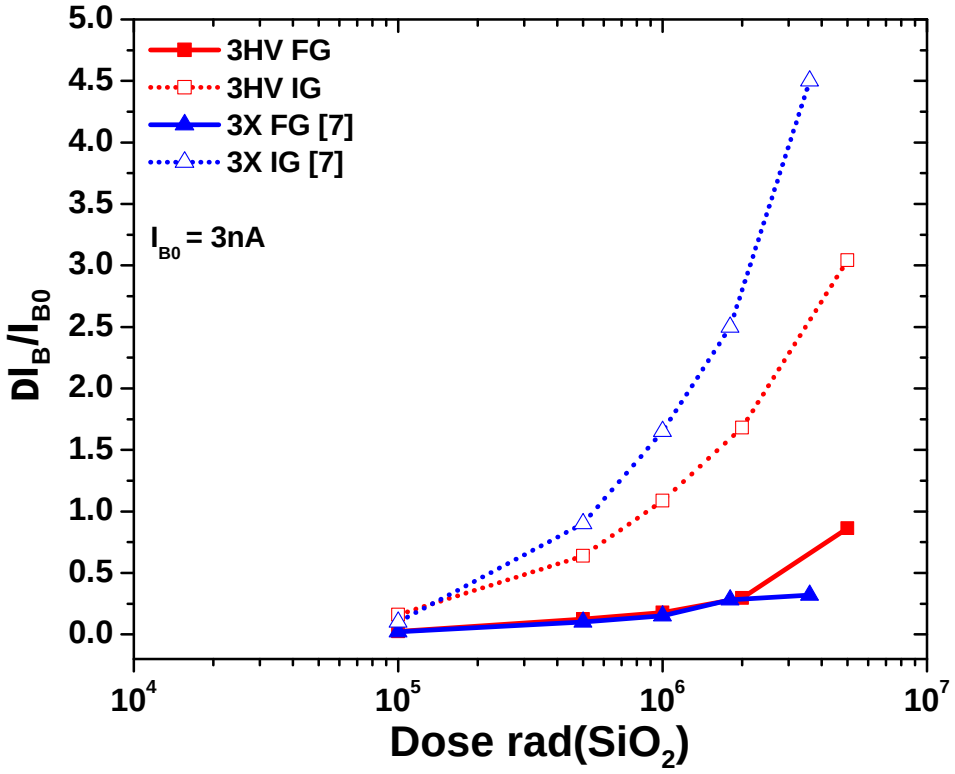


Figure 6.9: Excess normalized I_B for the PNP as a function of dose. The 3X technology is compared with the results for the 3HV platform for both forward and inverse-mode.

To see the impact of TID on β, the normalized β as a function of V_{BE} for three different doses along with the three different bias conditions is plotted on Fig. 6.10. A similar behavior as the NPN is observed, with the expected large change at low and medium injection, and an additional decrease at high injection. However, in the PNP case, the peak reduction in current gain is 20-40% larger than the NPN at higher doses, with the PNP showing a maximum reduction of approximately 85% at 5 Mrad(SiO_2). Similar to the NPN, the bias dependence is observable with the grounded condition showing the lowest reduction and Bias 2 showing the largest reduction, thus, implying that there is a V_{CB} dependence. However, at 5 Mrad(SiO_2), it is clear the bias dependence is no longer significant which likely indicates that it does saturate past a certain dose. Once again, J_C showed minimal change ($< 5\%$) at grounded condition but showed a more profound difference at the other two bias

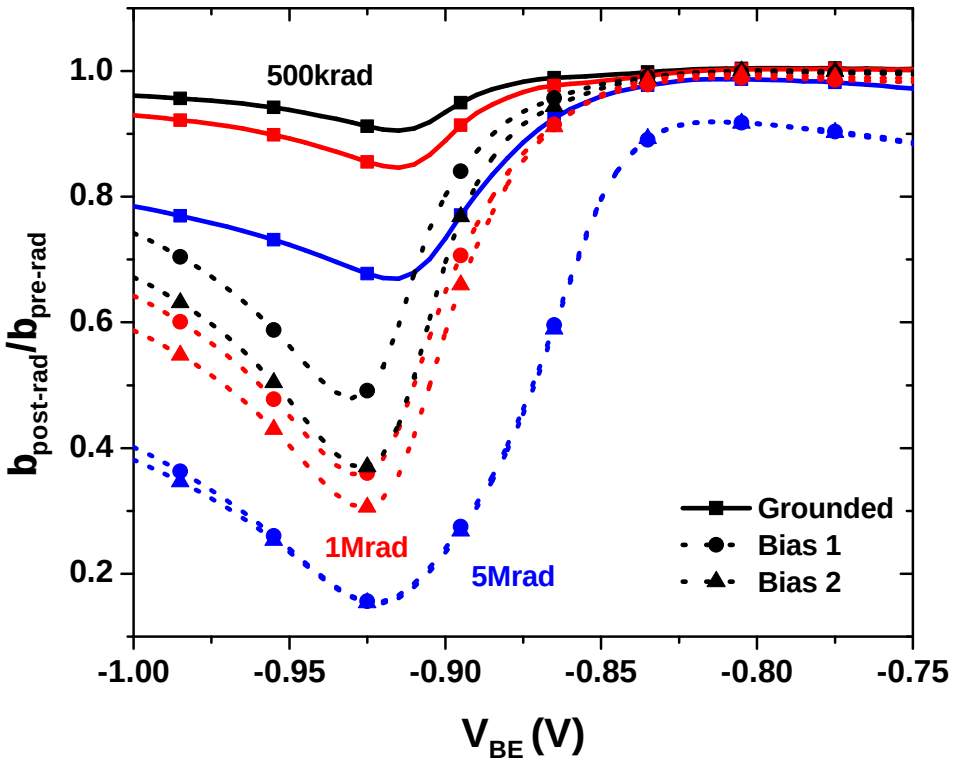


Figure 6.10: Normalized current gain (grounded condition, Bias 1, and Bias 2) post- and pre-radiation for the PNP as a function of V_{BE} for the following cumulative doses: 500 krad(SiO_2), 1 Mrad(SiO_2), and 5 Mrad(SiO_2). Solid lines are grounded condition while dotted lines correspond to Bias 1 and Bias 2.

conditions with accumulated dose, however, J_B was still the limiting factor and the normalized I_B is plotted on Fig. 6.11. The same trend as the NPN is observed, but the raw increase in I_B at large V_{BE} is significantly higher (>5X increase compared to 2X increase for NPN), which is consistent with the current gain reduction.

The low injection change in both forward and inverse mode for the PNP is compared for all the the bias conditions in Fig. 6.12. Similar to the NPN, minimal differences are observed between the grounded and other two bias conditions for forward-mode operation, which is logical, since the induced electric-field shouldn't affect the EB spacer. A more significant difference is observed, however, in the inverse-mode operation. The trend once again is similar to the NPN, but the raw values are significantly higher. The bias dependence is also very clear as a higher V_{CB} shows more than a 2X increase in base current at larger doses. This implies that with higher bias,

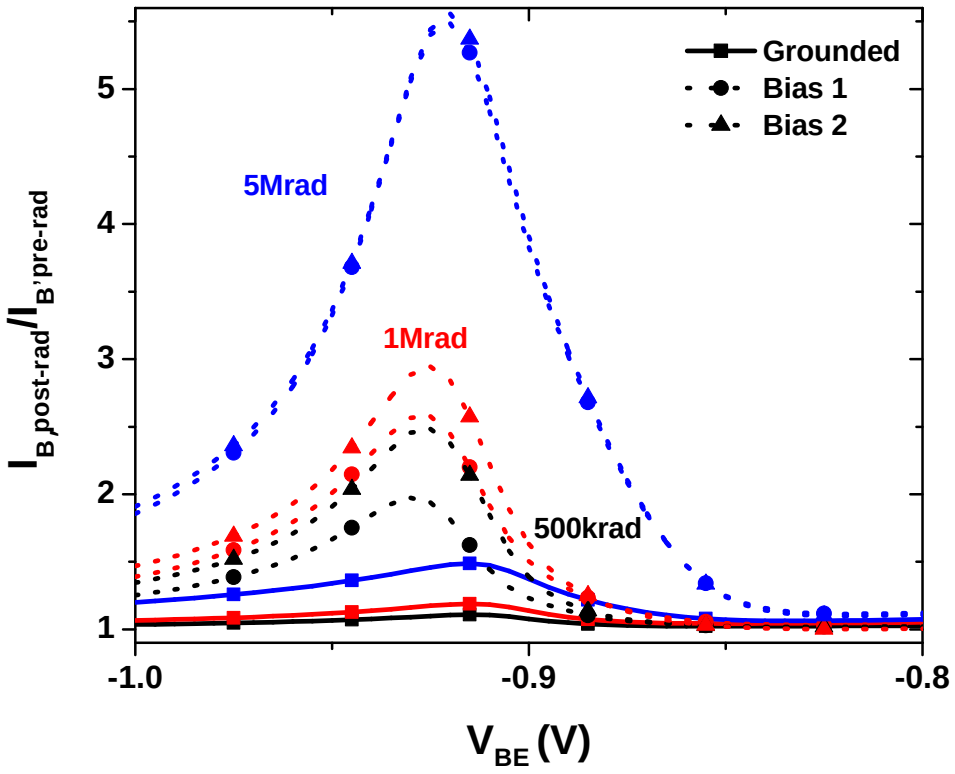


Figure 6.11: Normalized I_B (grounded condition, Bias 1, and Bias 2) post- and pre-radiation for the PNP as a function of V_{BE} for the following doses: 500 krad(SiO_2), 1 Mrad(SiO_2), and 5 Mrad(SiO_2). Solid lines are grounded condition while dotted lines correspond to Bias 1 and Bias 2. Only the high-injection bias is shown.

there is a significantly higher amount of interface traps along the Si-SiO_2 interface, which leads to the higher SRH recombination leakage current. Similar to the NPN case, the electric-field helps to more efficiently separate the generated electron-hole pairs (EHP) in the STI and generates more interface traps from the secondary reaction [41]. While the polarity of the field is different compared to the NPN, TCAD simulations still show that the field near and around the STI are oriented in an advantageous direction for EHP separation. The primary difference in the electric-fields between the NPN and PNP is whether they point towards the top or bottom of the STI. It is also likely that there are some structural differences between the NPN and PNP contributing to the differences in leakage current.

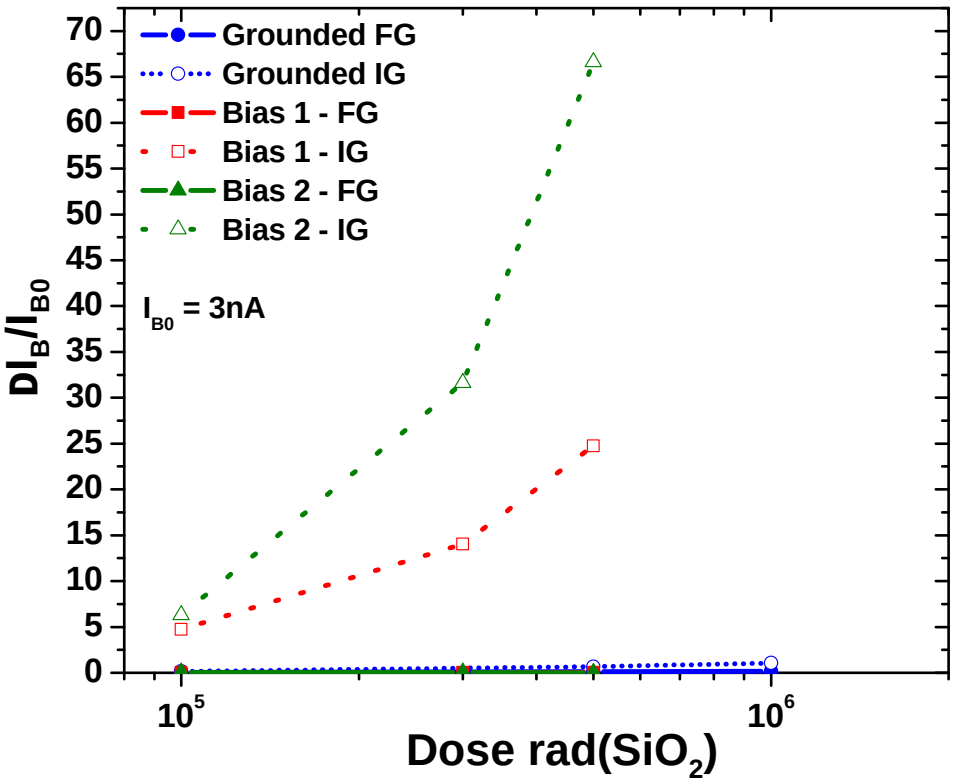


Figure 6.12: Excess normalized I_B for the PNP as a function of dose for forward and inverse-mode grounded and other bias conditions.

6.3 TCAD Simulations

In order to better understand both the general TID results and the observed high-injection phenomenon, calibrated TCAD models were built for the both the NPN and PNP. Fig. 6.13 illustrates the calibrated 2-D TCAD simulated Gummel compared with the measured data. Along with the Gummel, the devices were also calibrated to match f_T, f_{max}, and BV_{CEO} to ensure the best accuracy of the collector doping profile. The collector doping in particular is extremely important in the following simulations, since the STI interface traps play a crucial role in the high-injection response and therefore, accurate collector doping ensures the proper space charge region in the vicinity of the STI.

TID is responsible for positive fixed charge in the oxides and interface traps along

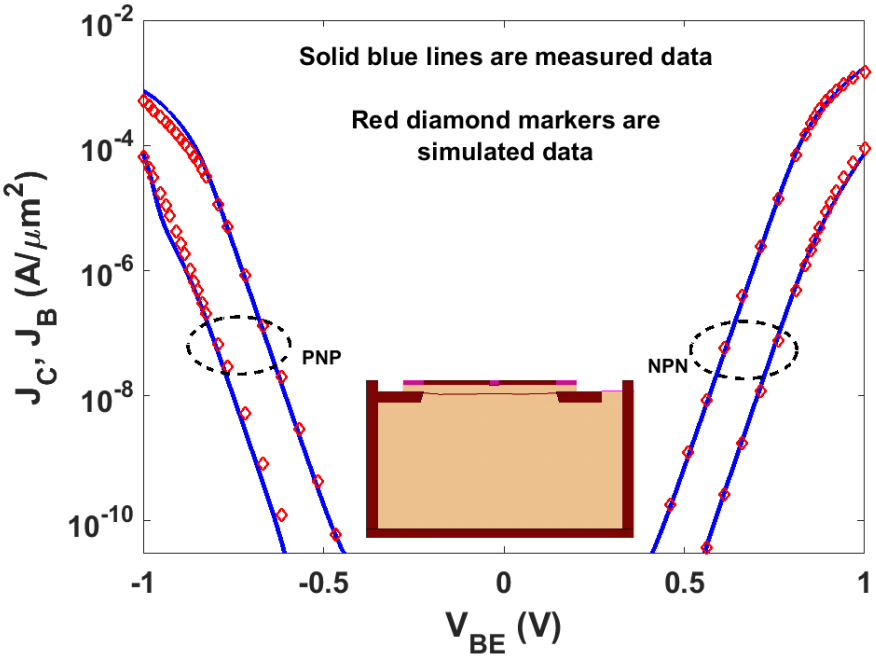


Figure 6.13: Measured Gummel for both NPN and PNP illustrated with solid blue line with simulated TCAD model Gummel overlaid on top with red diamond markers. A 2-D cross-section of the device used in TCAD simulations is also illustrated at the bottom.

the oxide/Si interface [41]. Therefore, in order to accurately simulate the TID response, the following steps were performed: 1) add positive fixed charge inside oxides and along the oxide/Si interface; 2) add interface traps (mid-band) along oxide/Si interface (ranging from 10^{10} cm^{-2} - 10^{12} cm^{-2}). The main oxides that were targeted were EB spacer oxide between the emitter and base contact, STI oxide between the base and collector contact, and the underlying BOX beneath the subcollector.

From initial TCAD simulations, it was concluded that charge or interface traps along and inside the BOX had no effect on the electrical response of these devices. Both NPN and PNP showed a similar response and thus no accumulation or depletion generated through fixed charge in the thick BOX had any impact on the collector or base current. This is not a surprising result, since the BOX is too far from the base to have any impact on the base current and any accumulation or depletion region will have minimal impact on the collector current due to the very high doping in the

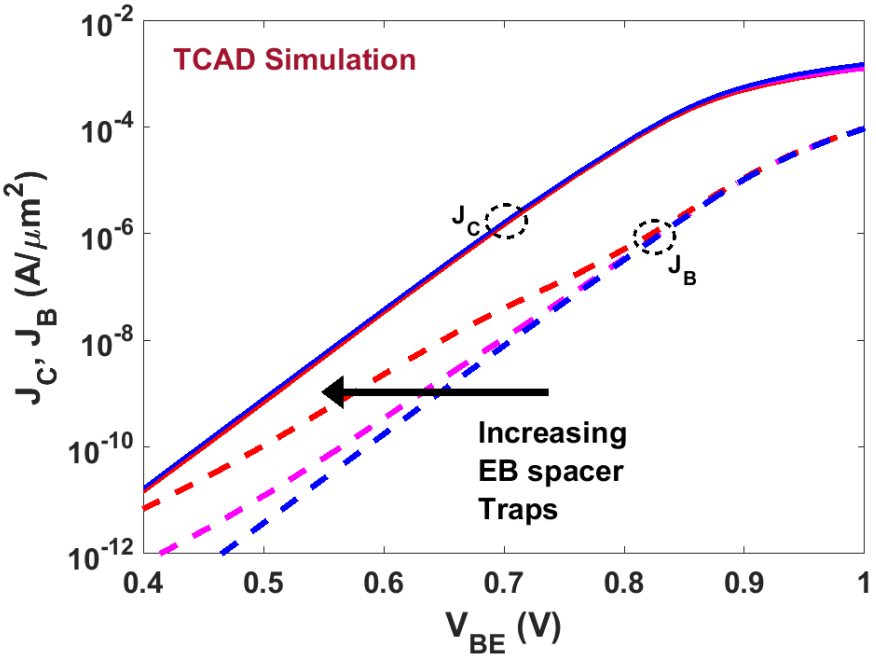


Figure 6.14: TCAD simulated forward-mode Gummel with increasing EB spacer interface traps.

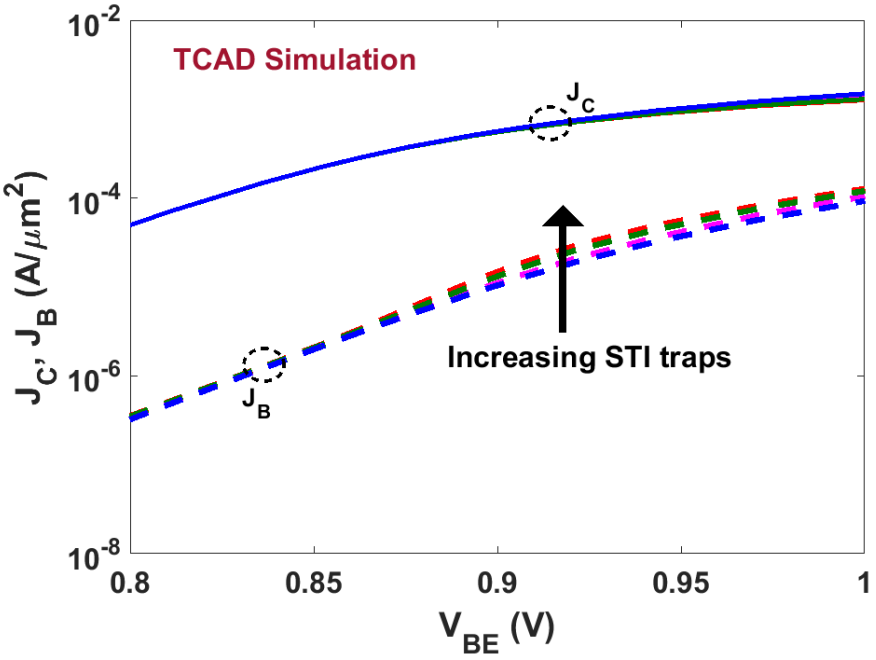


Figure 6.15: TCAD simulated forward-mode Gummel with increasing STI interface traps. Only the high-injection region is shown.

subcollector.

Interface traps and fixed charge were subsequently added to the EB spacer oxide. Fixed charge alone did not significantly alter the Gummel response of either the NPN or PNP supporting the assertion from the measured results indicating that charge accumulation in the EB spacer was not enough to cause a significant change to the emitter area [44]. Interface traps, however, showed a strong effect on the Gummel response, especially at low injection. This is more clearly illustrated in Fig. 6.14 which illustrates the effect of increasing interface trap concentration. This is classical behavior seen in other SiGe HBT platforms [33].

The STI region was examined next via simulations for its effect on the total TID response. Similar to the EB spacer, fixed charge alone showed no discernible difference in the Gummel response. Interface traps were then investigated. It is well-known from literature that STI interface traps are known to cause excess base leakage current when a SiGe HBT is operated in inverse mode [33]. Similar to Fig. 6.14, the same trend was observed in the inverse Gummel with increasing concentrations of STI interface traps.

However, the more interesting aspect of adding STI interface traps was found in the forward Gummel response. For increased emphasis, only the high-injection Gummel response with the addition of STI interface traps is shown in Fig. 6.15. The arrow indicates increasing interface trap concentration. Surprisingly, the high-injection response simulated is identical to the observed trend seen in Fig. 6.5 and Fig. 6.11. While only the simulated NPN Gummel is shown in Fig. 6.15, the PNP showed a similar behavior in simulations. The implication here is that at high injection, interface traps along the STI start to exert a strong impact on the current gain. While STI interface traps do show the same high-injection behavior, it is important to eliminate other possible sources. Through simulations, it was also observed that bulk traps in the thick collector exhibited a similar effect but considering X-rays generally do

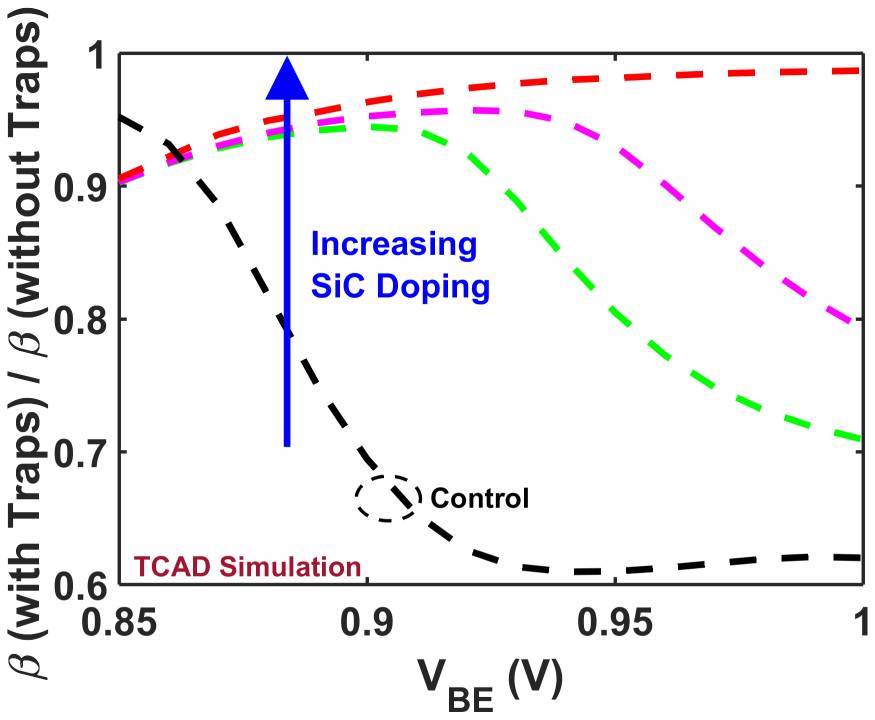


Figure 6.16: TCAD simulated forward-mode ratio of current gain with and without STI interface traps as a function of V_{BE} for three different SIC profiles and one control. Only high-injection region is shown.

not produce bulk traps in silicon, it can be ruled out. Interface traps at the Si/SiGe interface is also known to cause a similar effect, as detailed in [99, 100]; however, X-ray generated ehp in oxides should not be capable of creating traps at this growth interface.

Since this effect is observed at high injection, where heterojunction barrier and resistance effects can dominate in SiGe HBTs, it is important to understand the underlying mechanism. Barrier effects are unlikely to be the source given the nature of TID. Therefore, resistance degradation was investigated further. Emitter resistance perturbation was already ruled out due to the minimal change in collector current. Base resistance perturbation can also be ruled out given that an increase or decrease in base resistance will cause a shift in the same direction in both base and collector current, whereas, measured data indicates an increase in base current with a very small decrease in collector current. Collector resistance perturbation, on the other

hand, is consistent with the measured results. TCAD simulations indicate that an increase in the collector resistance shows a marked increase in the base current while showing minimal reduction in the collector current.

Given that this has not been observed before in SiGe HBTs, we aimed to investigate why this was observed in the present platform. Considering that the biggest difference between the technology used in this work and other SiGe HBTs tested for TID in literature is the BV_{CEO}, the impact of collector doping was investigated. In order to test how much the collector doping affects this high-injection phenomenon, TCAD simulations were performed with different selectively implanted collector (SIC) profiles. The control SIC profile used for comparison was the profile that was calibrated to measured data in Fig. 6.13. Three other extra SIC profiles were created with essentially increasing overall collector doping. The subcollector doping itself was left untouched. Basically, with each successive profile, the device becomes closer to a "typical" high-speed SiGe HBT. The STI interface trap concentration was held the same for all four profiles.

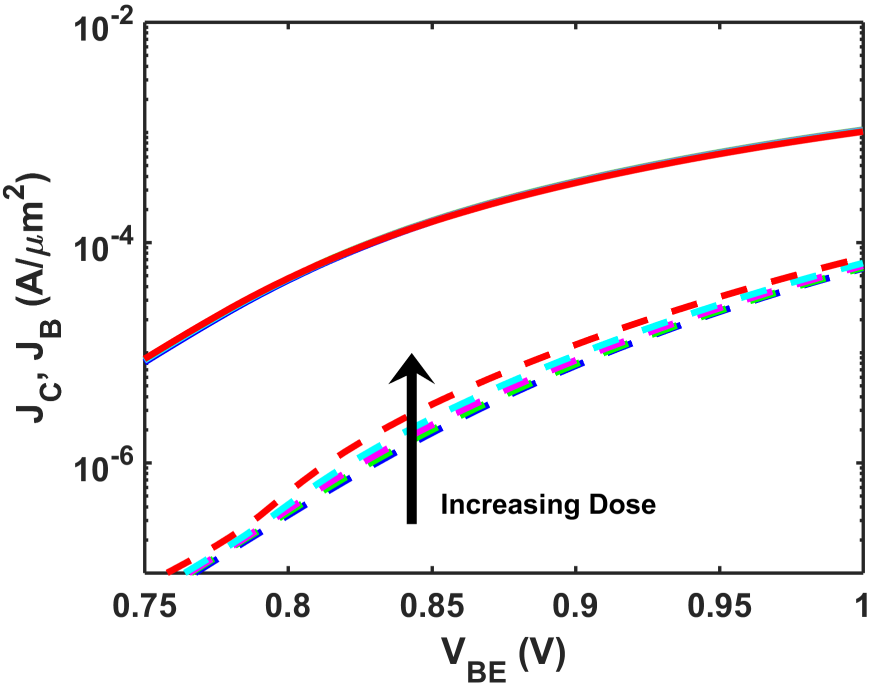
The high-injection current gain response of these three different SIC profiles along with the control profile are plotted in Fig. 6.16. Each curve represents a single profile and it shows the current gain with STI traps normalized to the current gain without STI traps. The arrow indicates the direction of increasing collector doping. Essentially, with increasing collector doping, the high-injection current gain degradation weakens significantly. While it is not shown, the collector current does change slightly with each SIC profile since an increase in collector doping will have a significant effect on the overall collector resistance resulting in the more apparent increase in the overall collector current. However, by normalizing the current gain for each profile, the results in Fig. 6.16 only illustrate the net change due to STI traps rather than differences rising from doping changes. The result is intuitive, since an increase in collector doping effectively reduces the base-collector space charge region, and thus

exposing less surface area of the STI in the depletion region. While it is a fairly different technology, the work in [101] utilizing a thin-film SOI device, illustrated a similar high-injection behavior with mixed-mode electrical stress. Similar to what is observed in the present work, the effect was only observed for the device with a lightly doped collector.

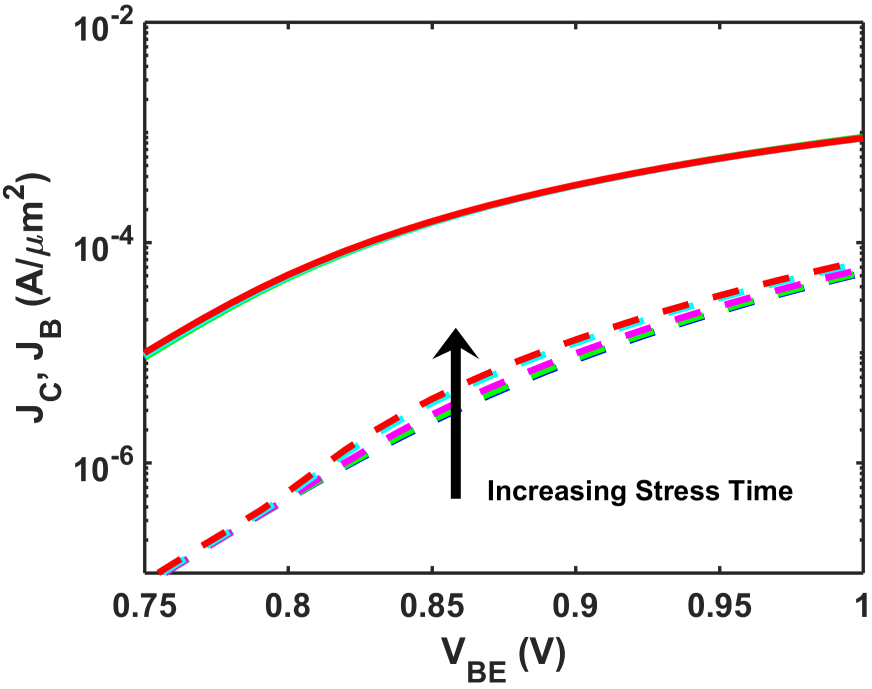
6.4 TID and Mixed-Mode Stress Comparison

In order to confirm independently whether this high-injection phenomenon is related to STI interface traps, mixed-mode electrical stress was performed [76]. For the stress, the devices were biased in a common-base configuration with a constant V_{CB} and J_E. Similar to studies before that have related radiation induced damage to mixed-mode stress damage, an attempt here was made to replicate the observed high-injection phenomenon with a separate stress measurement [80, 102]. Using an identical device with the same geometry, a stress condition with V_{CB} greater than BV_{CBO} and moderate I_E ($< J_{C,Kirk}$) was used to maximize impact ionization. Ideally, mixed-mode stress should induce a high concentration of interface traps along STI and EB spacer and therefore, if a similar high-injection effect is observed then it supports the notion that STI interface traps are the main driving force.

The results are illustrated in Fig. 6.17. Fig. 6.17(a) illustrates the high-injection behavior from TID with an all-grounded bias condition while Fig. 6.17(b) illustrates the high-injection behavior with mixed-mode stress. The arrow in Fig. 6.17(a) indicates increasing dose while the arrow in Fig. 6.17(b) indicates increasing stress time. It can be seen that the trend is similar between both indicating a strong correlation between STI interface traps and a high-injection current gain degradation. While only the NPN results are shown in Fig. 6.17, both NPN and PNP were stressed using the same methodology and both showed a similar response. Even from a mixed-mode



(a)



(b)

Figure 6.17: A comparison between (a) forward-mode Gummel with increasing dose from 100 krad(SiO_2) to 5 Mrad(SiO_2) and (b) forward-mode Gummel under mixed-mode stress with increasing time from 100 s to 10,000 s.

electrical stress perspective, this high-injection current gain degradation was not observed in other platforms with significantly higher collector doping (> 200 GHz f_T), thus lending credence to the collector doping dependence of this observed TID effect. It is worth noting that the collector resistance for the mixed-mode stressed device was measured both before and after stress using the method in [103] and it showed approximately a 7X increase, consistent with the data.

6.5 Summary

This work has investigated the TID response of a high-voltage complementary SiGe on SOI technology, and illustrates both the forward and inverse mode TID response. We have looked at the bias (V_{CB}) dependence on the TID response and surprisingly, bias has a strong impact on the inverse mode leakage current. Additionally, a novel current gain degradation phenomenon is observed in forward-mode operation at high injection which is correlated with the creation of interface traps at the STI oxide. However, like other SiGe HBTs, these high-voltage devices do show similar robustness to TID at low to moderate doses within the normal operating conditions (peak β or peak f_T).

CHAPTER 7

TEMPERATURE DEPENDENCE OF SEE

Silicon-germanium heterojunction bipolar transistors (SiGe HBTs) have been shown to possess very favorable properties in a variety of extreme environments [12]. From a radiation perspective, both total dose effects and single-event effects (SEE) in SiGe HBTs have been reported in the literature [39]. However, an aspect of extreme environments that has not been explored as thoroughly for SiGe HBTs is the intersection of radiation and temperature. The general behavior of SEE in SiGe HBTs is reasonably well understood, but the exact measured temperature dependence of SEE has never been reported. From a high-temperature application perspective, an arena of growing importance to the aerospace community, initial research on both the performance and reliability of SiGe HBTs at elevated temperatures clearly indicates that SiGe HBTs have significant potential for use in such challenging environments [1, 3]. However, at present no data exists on an envisioned application that involves simulataneous exposure to both high temperatures and radiation, and which would include, for instance, planetary exploration missions and particle detector facilities [29].

To investigate the effects of temperature on the SET response of SiGe HBTs, a complementary high-voltage (>30 V) SiGe-on-SOI technology was utilized [77]. These devices are markedly different from typical SiGe platforms, since they were optimized for high-breakdown voltage and not necessarily high speed. Thus, they find a larger role in precision analog and high-voltage applications than do other more traditional RF-optimized SiGe HBTs. These devices also contain a buried oxide that isolates the collector from the substrate, which greatly reduces the collector-substrate junction leakage current at higher temperatures. The purpose of the present work is

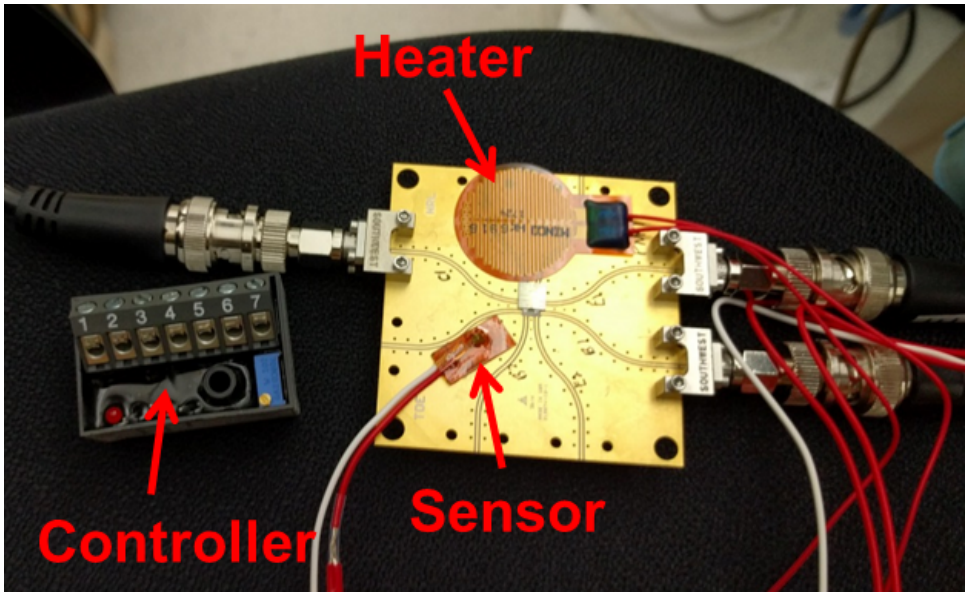


Figure 7.1: Test setup for high-temperature SET testing.

to characterize the transient response of this high-voltage SiGe HBT platform, and use its favorable high-temperature properties to investigate the combined effects of temperature and radiation on the transient response. Additionally, this work explores the role that thermal effects play in the transient response, not only in this particular SiGe technology, but for other SiGe HBT technologies, even those optimized for low voltage and high speed.

7.1 Experimental Setup

NPN and PNP SiGe HBT structures with the same emitter geometry were packaged and wirebonded on a printed circuit board (PCB). To expose devices to laser light for transient testing, the backside of the PCB under the die was left exposed. The devices were biased using Keithley 2400 source measure units (SMUs). A Tektronix DPO71254, 16 GHz, 50 GS/sec, real-time oscilloscope, was used to measure the device transients. Transients were induced via two-photon absorption (TPA) process using a 1260 nm wavelength optical pulse, which results in $\approx$ 1 μm full width at half maximum (FWHM) spot size [104].

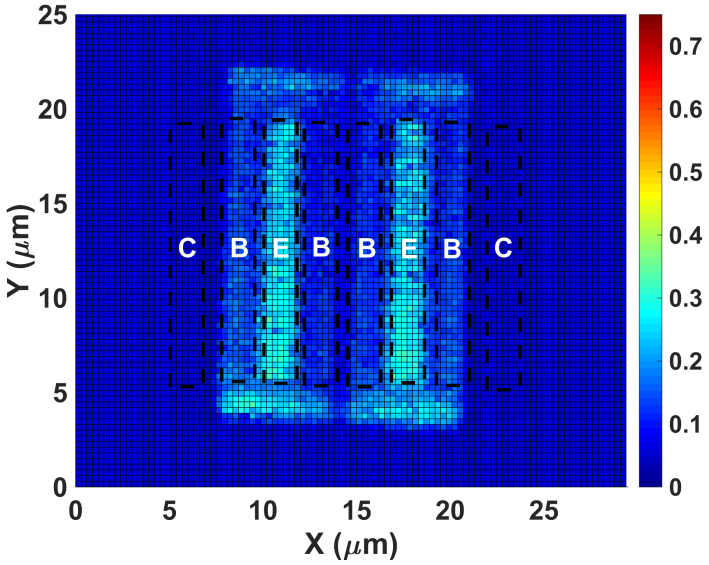
Three different emitter current density (J_E) bias conditions were used to test the transient response of the NPN and PNP SiGe HBTs, including: a low J_E bias condition (10 $\mu A/\mu m^2$), a moderate bias condition (50 $\mu A/\mu m^2$), and a high bias condition (100 $\mu A/\mu m^2$). The low J_E bias condition was used to ensure low power dissipation, while the high J_E bias condition was used to simulate an actual high-power operating condition close to peak f_T bias. As the NPN and PNP devices have different collector currents (I_C) for the same V_{BE}, a common-base biasing configuration was utilized. In this case, the base was grounded while the emitter was tied to a constant current source, and the collector voltage was manually tuned with a voltage source. To maximize the peak amplitude of the transients, raster scans in all three spatial directions were performed across the entire active region of the devices. Using the raster scan data, the laser was focused on the most sensitive region, which also happens to be the emitter center. All subsequent transient measurements were made by focusing on this particular sensitive region.

For high-temperature transient measurements, the setup illustrated in Fig. 7.1 was used. A Minco heater coil and thermal sensor were used for heating up the board and measuring the temperature, respectively. The heater coil and thermal sensor were affixed to the PCB using an acrylic adhesive. A PID controller was implemented using MATLAB, and a temperature accuracy of $\pm$ 0.5°C was achieved.

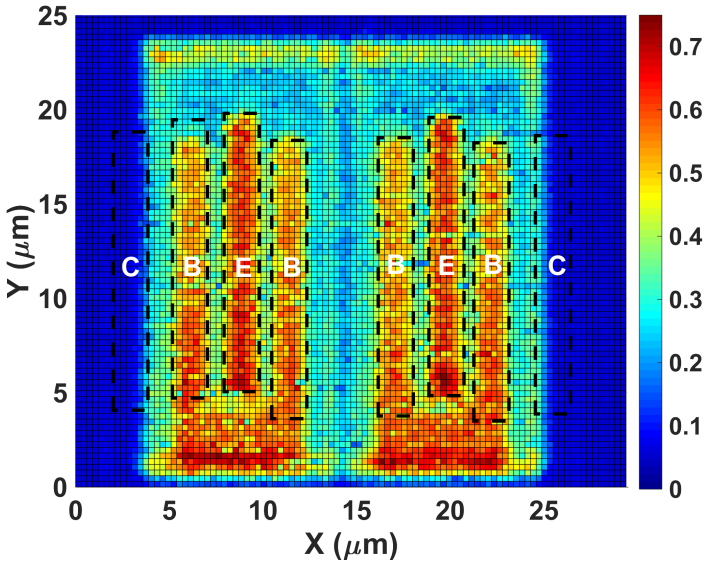
7.2 Results

7.2.1 NPN and PNP Comparison

2-D raster scans highlighting positional dependence of the collector transient peak amplitudes for both the NPN and PNP SiGe HBTs are shown in Fig. 7.2. The raster scans were performed at a similar bias condition for both devices (J_E = 10 $\mu A/\mu m^2$ and V_{CB} = |1 V|). This particular bias condition was chosen since it is is near peak current gain (β) and as such, it is a relevant bias condition for many analog circuit



(a) NPN Collector Transient Peaks (mA)



(b) PNP Collector Transient Peaks (mA)

Figure 7.2: 2-D raster scans for NPN and PNP devices highlighting the magnitude of the collector transient peak amplitudes with an applied bias of $\mathbf{J_E} = |\ 10\ \mu\mathbf{A}/\mu\mathbf{m}^2|$ and $\mathbf{V_{CB}} = |1\ \mathbf{V}|$. Results are for 24°C.

applications. Additionally, no self-heating should be observed in this bias condition, and thus the results should not be influenced by any temperature effects.

There are two key observations worth highlighting in the raster scans shown in Fig. 7.2. First, the overall area for the PNP SiGe HBT is larger than the overall area for the NPN SiGe HBT. However, while the overall active area for the PNP

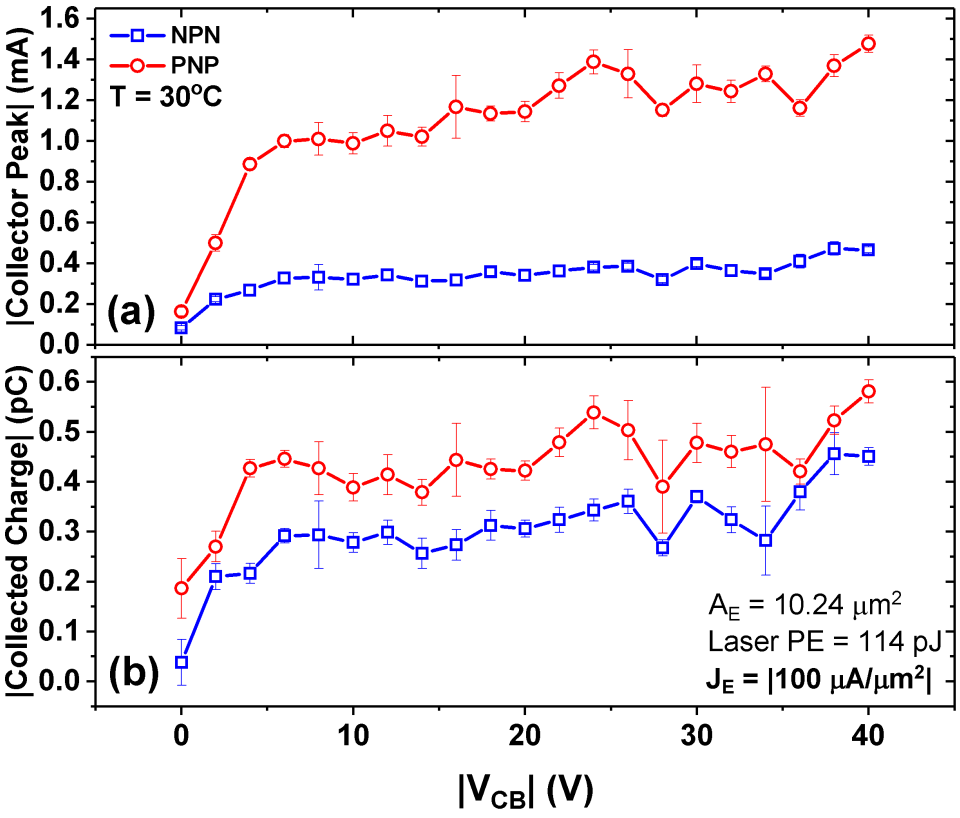


Figure 7.3: (a) Collector transient peak amplitude and (b) Collector collected charge as a function of V_{CB} for both NPN and PNP. Both results are for an ambient temperature of 30°C.

device is larger, both the NPN and PNP devices have similar emitter widths. The vertical distance from the top of the emitter stack to the bottom of the buried oxide layer (BOX) is also the same for both devices. The second key observation is the difference in transient peak magnitude between the NPN and PNP SiGe HBTs. The peak transient collector current observed in the NPN device is |0.3 mA|, while for the PNP device it is |0.7 mA|, over 2X larger.

To better understand the differences in transient response between the NPN and PNP SiGe HBTs, the collector transient peak amplitude and collected charge for a variety of V_{CB} bias conditions were analyzed. Fig. 7.3(a) shows the collector transient peak amplitude as a function of V_{CB} while Fig. 7.3(b) shows the collected charge as a function of V_{CB} at 30°C. Both the NPN and PNP devices show a similar V_{CB}

dependence for both the peak amplitude and collected charge, where a sharp increase is observed after V_{CB} of 0 V, and then a relatively small increase with subsequent V_{CB} values. From a V_{CB} of 0 - 5 V, close to 300% change in both transient peak amplitude and collected charge is observed, although only a 50% change is observed from 5 - 40 V. The increase in peak amplitude with increasing V_{CB} can be explained by using the simple model for SET current described by

$$I(t) = -qN\mu' E_0(e^{-\alpha t} - e^{-\beta t}) \tag{7.1}$$

where μ' is the average mobility, N is the total injected charge, E_0 is the electric field, $1/\alpha$ is the collection time constant of the junction, and $1/\beta$ is the time constant for establishing the initial ion track [57, 105]. An increase in V_{CB} results in an increase in the electric field, which should increase the transient peak amplitude. Mobility, on the other hand, reduces at large fields. TCAD simulations were performed to analyze the rate at which the electric field and mobility change with V_{CB}. The Canali mobility model was used to properly model the high-field behavior [106]. The simulated $\partial E_0/\partial V_{CB}$ and $\partial \mu'/\partial V_{CB}$ is plotted as a function of V_{CB} in Fig. 7.4. The electric field clearly changes at a faster rate than the mobility does for all V_{CB}. In fact, from around 10 V to 35 V, the rate at which mobility changes approaches zero (i.e. the mobility starts to saturate). The increasing transient peak amplitude with increasing V_{CB} in Fig. 7.3 also strongly implies that the electric field dominates over the mobility dependence. The change in transient duration was negligible at large V_{CB}.

The overall results clearly indicate that, for a similar bias condition, the PNP transient peak amplitudes are significantly larger (more than a 2-3X increase). This result is different from previously reported results for complementary SiGe HBTs from a low-voltage, high-speed technology platform, which found the PNP device to be less sensitive to transients than the NPN device [50, 107]. There are two main

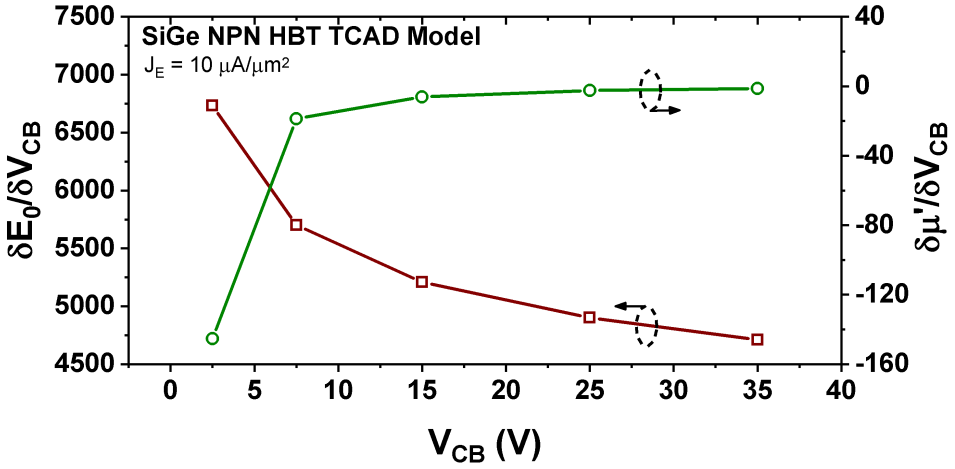


Figure 7.4: TCAD simulated rate change of the electric field (E_0) and average mobility (μ') as a function of V_{CB}.

differences between the present SiGe platform and the platforms used in [50, 107]: the higher breakdown voltage, and the difference in size between the NPN and PNP devices (the work in [50] is also non-SOI). To achieve the higher breakdown voltage for the devices used in this work, a thicker and lightly doped collector is required. The presence of this lightly doped collector has already been shown to impact the TID response of the present devices [2]. Additionally, since the PNP device is physically larger compared to an NPN device at fixed emitter geometry, there could also be a 3-D effect coming into play, which results in differences in the peak transients.

In order to emulate the effects of difference in charge collection volume on the SET response, a 3-D TCAD NPN model was developed. Three different structures were built with increasing total volume, and heavy-ion TCAD simulations were performed. The results are shown in Fig. 7.5, where the percent change in collector peak amplitude is plotted as a function of total volume. A 2X change in volume results in up to 32% increase in collector peak amplitude, while a 4X change results in a 60% increase in collector peak amplitude. From the 2-D raster in Fig. 7.2, the total sensitive area for the PNP device is approximately 2.5X larger than the NPN device. According to simulations, this should result in close to a 45% change in transient peak

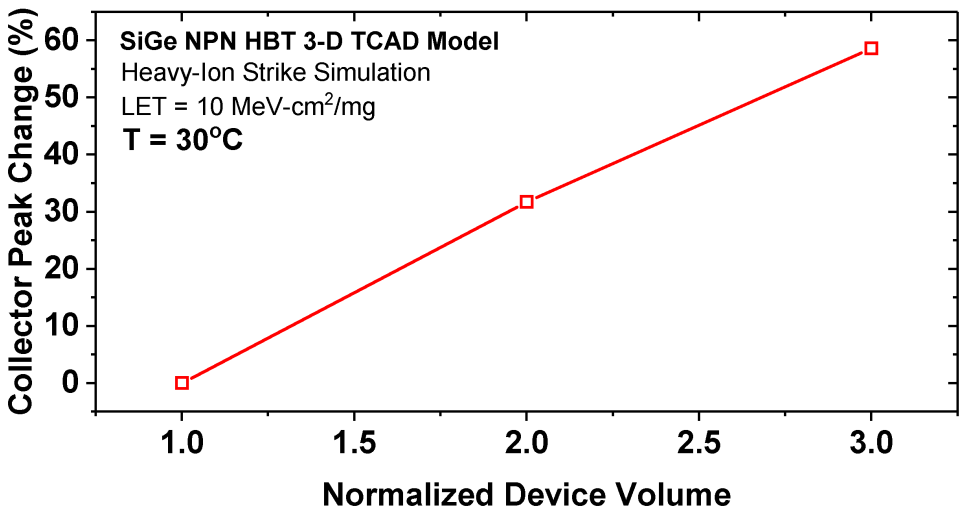
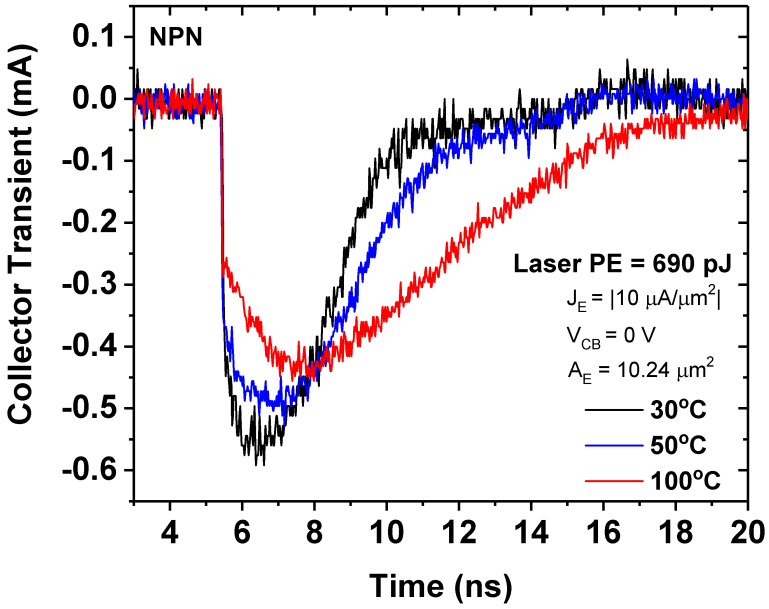


Figure 7.5: A 3-D TCAD simulated collector transient peak amplitude as a function of total device volume. Results are for 30°C.

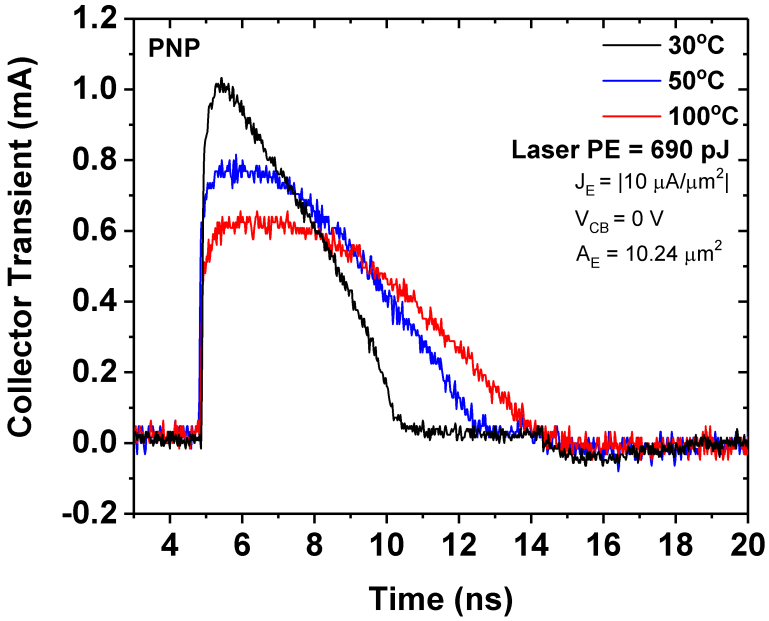
amplitude (everything else being held constant) between the NPN and PNP devices. However, this does not completely explain the observed differences between the NPN and PNP devices, since there is up to a 300% observed difference in transient peak amplitude. Another possible factor influencing the peak amplitude is the difference in peak germanium. It is well known that a PNP device requires a larger peak germanium content in order to achieve the same performance as a NPN device. A 10% increase in peak germanium was shown to increase the transient peak amplitude by more than 200% in [108]. A combination of higher collection volume and a difference in peak germanium likely results in the PNP device exhibiting a larger transient peak amplitude compared to the NPN device.

7.2.2 Temperature Results

Transients were measured at four different temperatures: 30°C, 50°C, 75°C, and 100°C. A pulse laser energy ranging from 100 pJ to 700 pJ was used for the measurements. Representative collector transients at a J_E of $|10\ \mu A/\mu m^2|$ and V_{CB} of 0 V, for both the NPN and PNP devices, from 30°C to 100°C, are shown in Fig. 7.6(a) and Fig. 7.6(b), respectively. Both the NPN and PNP devices show a similar trend with



(a) NPN



(b) PNP

Figure 7.6: (a) Measured collector transient peak amplitudes across temperature for (a) NPN and (b) PNP at V_{CB} of 0 V.

respect to temperature, resulting in a decrease in transient peak amplitude with increasing temperature, and an increase in the overall transient duration. Even though the transient peak amplitude decreases, the increase in the duration results in a slight

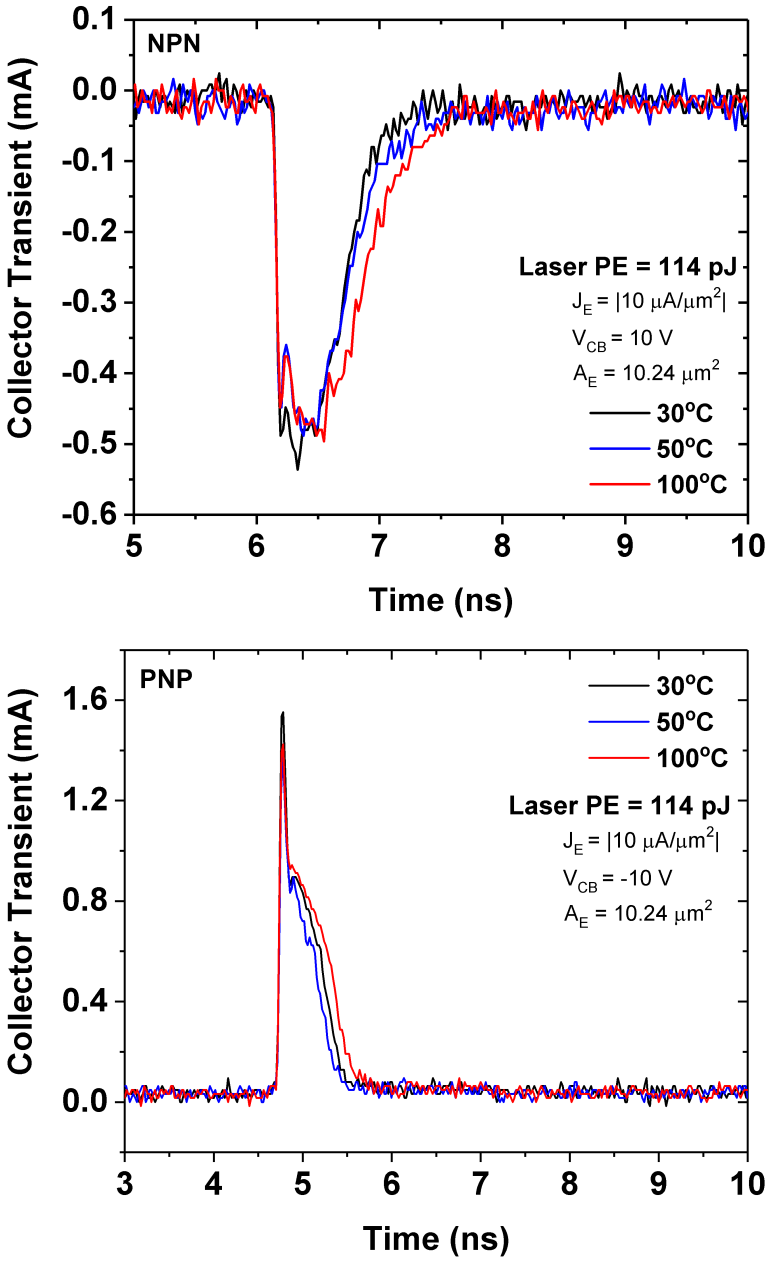


Figure 7.7: (a) Measured collector transient peak amplitudes across temperature for (a) NPN and (b) PNP at V_{CB} of |10 V|.

increase in the total collected charge. The observed differences in transient peak amplitudes between the NPN and PNP devices remains consistent across temperature for a V_{CB} of 0 V condition.

A clear temperature trend for the collector peak amplitude was identified for a V_{CB} of 0 V condition, but this temperature trend was not evident across all bias conditions. Once V_{CB} was increased from 0 V, the temperature dependence was no

longer observed. This is illustrated with representative collector transients across temperature in Fig. 7.7(a) and Fig. 7.7(b) at a V_{CB} of |10 V| for the NPN and PNP device, respectively. Unlike the V_{CB} of 0 V case, the transient peak amplitude shows very weak temperature dependence. The overall transient peak amplitude behavior for the two different V_{CB} is summarized in Fig. 7.8(a) and Fig. 7.8(b). It should be noted that there is a difference in pulse laser energy between Fig. 7.8(a) and Fig. 7.8(b). This was intentional, since a larger pulse energy was required to observe sufficiently large peak amplitudes in order to establish trends for a V_{CB} of 0 V condition. A lower pulse energy was used for a higher V_{CB}, since a higher pulse energy resulted in catastrophic device failure due to the significantly larger transient peak amplitudes (> 4 mA).

For a V_{CB} of 0 V condition in Fig. 7.8(a), up to 25% reduction in transient peak amplitude is observed for the NPN device, while up to 40% reduction in transient peak amplitude is observed for the PNP device. For a V_{CB} of 10 V condition in Fig. 7.8(b), the temperature dependence is significantly weaker compared to the V_{CB} of 0 V bias condition. Unlike the V_{CB} of 0 V bias condition, an increase in transient duration was not observed. This trend was seen for all V_{CB} conditions ranging from approximately 5 V to 40 V. This observation strongly implies that the internal electric field dominates the transient response with applied V_{CB}, rather than the ambient temperature.

Higher J_E bias conditions were also tested (not shown here), and they showed similar temperature trends. However, the peak amplitude was lower at a higher J_E condition compared to a J_E of 10 $\mu A/\mu m^2$. This is primarily due to the reduction in the peak electric field at the EB junction. Since a larger forward bias is required to get a larger J_E, the peak electric field at the EB junction is reduced.

The collected charge was also analyzed across temperature, and the results are shown in Fig. 7.9. Unlike for the temperature dependence for the collector transient peak amplitude, even at a V_{CB} of 0 V, there is no clear temperature trend observed.

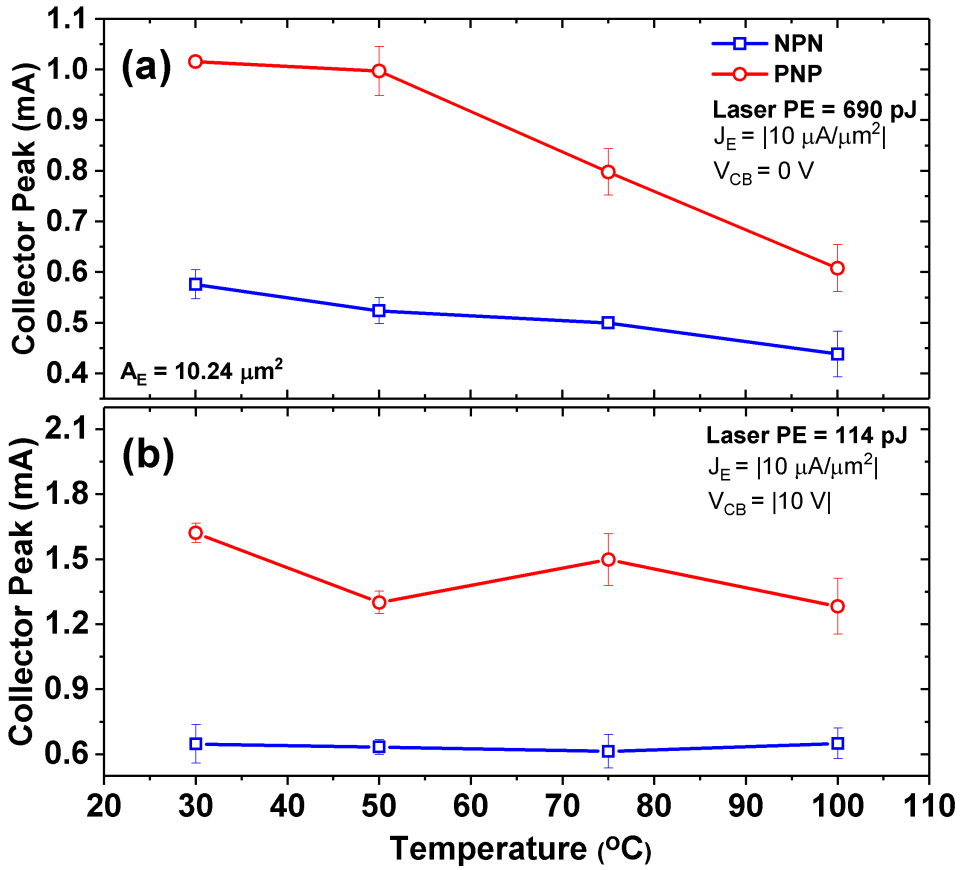


Figure 7.8: Collector peak amplitude as a function of temperature for NPN and PNP at (a) $V_{CB} = 0$ V and (b) $V_{CB} = 10$ V.

This relative lack of temperature dependence over this temperature range is similar to what was reported in [57] for an epilayer diode. An increase in V_{CB} (measured up to 40 V) also showed no observable temperature trend.

7.3 Analysis

While some of the measured results display a clear trend, it is important to decouple any potential optical effects associated with the laser that may influence the high-temperature results. Mainly, the laser power reaching the device could potentially change due to the reflections at the silicon-air interface. These reflections are dependent on the index of refraction of silicon, which increases slightly with increasing temperature [109]. The reflective loss at 24°C is approximately 30.80% and at 100°C,

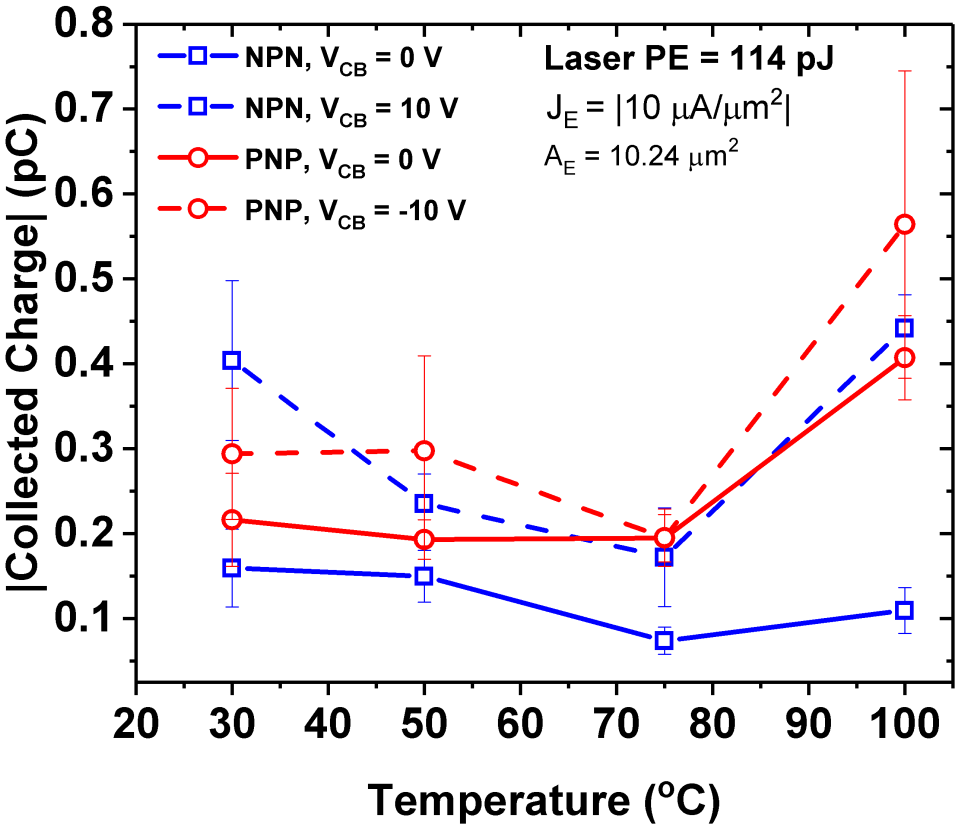


Figure 7.9: Collected charge as a function of temperature for V_{CB} = 0 V, and V_{CB} = 10 V for both NPN and PNP devices.

the reflective loss is 31.39%. Since there is less than 1% change in reflective loss, it can be assumed that there is no significant change in the laser power reaching the device.

Another potential source for the observed temperature dependence is the TPA absorption coefficient. To the best of the author's knowledge, there are no reported results for the temperature dependence of the TPA absorption coefficient. Data has been reported on the temperature dependence of the single photon absorption coefficient, and it was shown to increase with increasing temperature [110].

In order to definitively determine whether the measured transient peak amplitude's temperature trend at low V_{CB} originates from the intrinsic device, TCAD simulations were performed over the temperature range of interest. Calibrated 2-D TCAD models were constructed, and heavy-ion strike simulations were performed. A

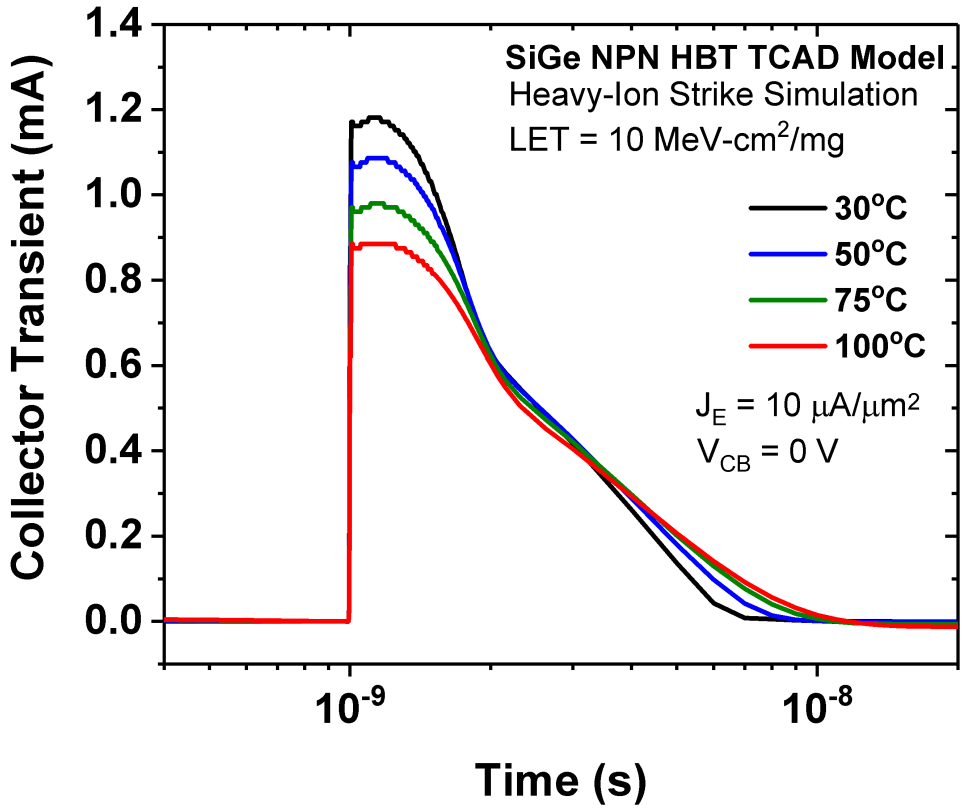


Figure 7.10: TCAD simulated heavy-ion strikes from 30°C-100°C.

2-D model was used rather than a 3-D model to reduce computational complexity. The simulation results for a NPN SiGe HBT at a V_{CB} of 0 V is shown in Fig. 7.10, and it does exhibit the observed trend of decreasing transient peak amplitude data with increasing temperature. Although it is not shown here, the PNP device simulation results all showed the same trend as the NPN results.

Further TCAD simulations were performed to better understand the temperature dependence of the transient peak amplitudes. The V_{CB} dependence in particular needed to be explored further. Fig. 7.11 shows the change in collector transient peak amplitude as a function of temperature for V_{CB} from 0 V to 20 V. Similar to measurements, V_{CB} of 0 V case shows the strongest temperature dependence, where approximately 30% reduction in transient peak amplitude is observed. However, with increasing V_{CB}, the temperature dependence becomes much weaker. At a V_{CB} of 20

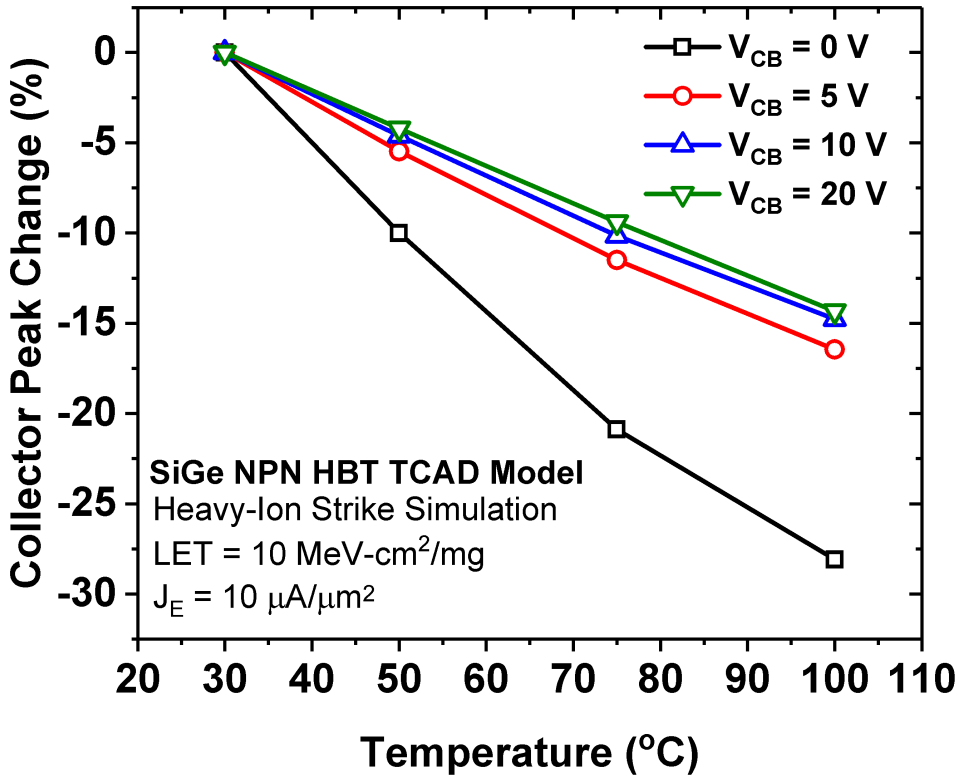


Figure 7.11: TCAD simulated percent change in collector transient peak amplitude from 30°C-100°C for V_{CB} from 0 V to 20 V.

V, less than 15% change in transient peak amplitude is observed. This weaker temperature dependence with increasing V_{CB} is similar to what was observed in Fig. 7.8.

The reduction in transient peak amplitude with increasing temperature at low V_{CB} can be explained by understanding the temperature dependence of eq. 7.1. The two key temperature dependent terms that strongly influence the transient peak amplitude are E_0 and μ'. While it is hard to measure the electric field directly, calibrated simulations can help understand the temperature dependence of the field. The peak electric field along the emitter center as a function of temperature was investigated in TCAD. The percent change in the peak electric field as a function of temperature for V_{CB} from 0 V to 40 V is shown in Fig. 7.12. A V_{CB} of 0 V condition clearly has a significantly stronger temperature dependence, where a 30% decrease in peak electric field is observed at 100°C. As V_{CB} increases, the temperature dependence of the electric field becomes weaker. For a V_{CB} of 40 V, there is less than

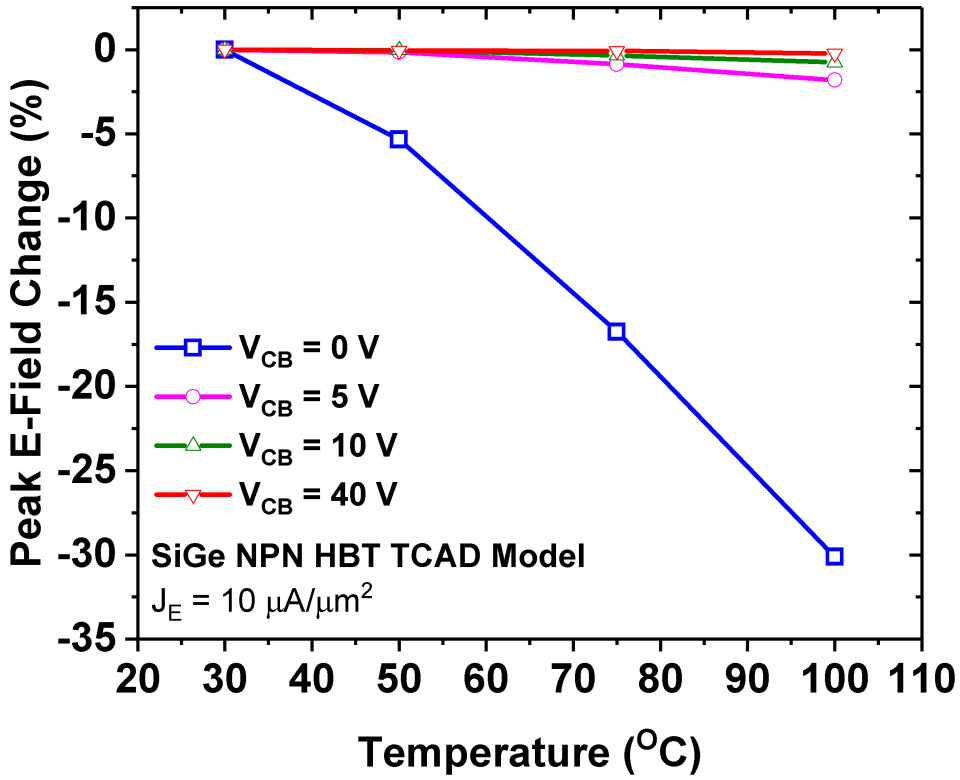


Figure 7.12: TCAD simulated percent change in peak electric field at the emitter center across temperature for V_{CB} of 0 V - 40 V.

a 0.5% change in the peak electric field. The strong reduction in the temperature dependence of the electric field partially explains why there is a lack of temperature scaling for the transient peak amplitude at higher V_{CB} in Fig. 7.8.

The other key temperature dependent parameter to be explored is the mobility. An average mobility value along the charge track as a function of temperature was found by integrating both the electron and hole mobility. Fig. 7.13 shows the percent change in mobility from 30°C-100°C as a function of V_{CB}. The reduction in mobility with increasing temperature is fairly intuitive, since higher temperatures are known to cause an increase in the resistivity of silicon due to increased carrier scattering. Similar to the peak electric field, the percent change in mobility with increasing V_{CB} becomes smaller. Even though the reduction is not as large as what is observed for the electric field, there is still a little over 10% reduction in the change in mobility at large V_{CB} values.

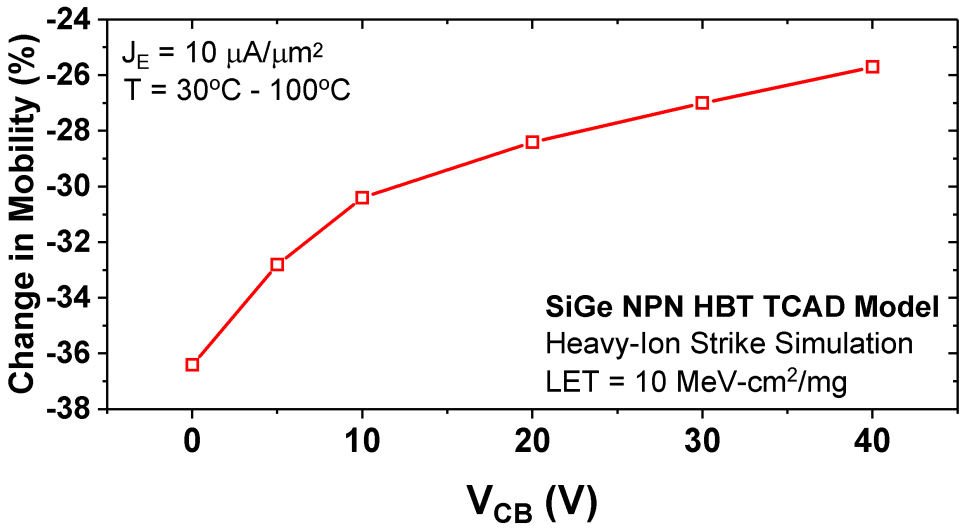


Figure 7.13: TCAD simulated average mobility percent change from 30°C-100°C as a function of V_{CB}.

While the simulation results still show at least a 15% change in transient peak amplitude at higher V_{CB} as a function of temperature, this was not observed in the data. The discrepancy likely suggests that the observed transient peak amplitude temperature dependence in the data is dominated more by the electric field than any change in the mobility. This could potentially be explored further by increasing the temperature range of the measurements. At temperatures higher than 100°C, one would expect the mobility to drop much further, and if a clear decrease in transient peak amplitude is observed at higher V_{CB}, it would indicate that a larger reduction in mobility is required to cause a significant change in the transient peak amplitude response.

Finally, the temperature dependence of the collected charge needs to be better understood. The total collected charge can be separated into two distinct components: drift and diffusion [57, 59]. The charge collected by drift is dominated by the carrier velocity, which has been shown to decrease with increasing temperature. However, the charge collected through drift is usually on a significantly smaller time scale compared to the total duration of the transient [59]. The charge collected through diffusion is

observed in the longer tail, which contributes to the majority of the duration of the transient. This diffusion behavior is mainly controlled by the minority carrier diffusion length. The diffusion length is dependent on both the ambipolar diffusion coefficient, and the minority carrier lifetime [57]. The diffusion coefficient is known to decrease with increasing temperature, but there is no general accepted temperature dependence for the minority carrier lifetime. A typical power law dependence is assumed for the purposes of this work, which gives the minority carrier lifetime a positive temperature coefficient [111]. Since the diffusion coefficient decreases with temperature, and the minority carrier lifetime increases with temperature, the minority carrier diffusion length has an overall weak temperature dependence, which is consistent with the lack of temperature dependence that is observed in Fig. 7.9 and in [57].

The temperature dependence can also be understood from eq. 7.1, where the diffusion tail is modeled by the two exponential terms, α and β. β is not expected to change significantly with temperature. The α, collection time constant of the junction, is inversely proportional to mobility and directly proportional to the electric field. As shown previously, the mobility and field become more temperature independent at large V_{CB}, which makes α weakly temperature dependent, and thus making the total collected charge also weakly temperature dependent.

The charge collection process is additionally related to the depletion region in the device. With increasing V_{CB}, the CB junction depletion region extends deep within the device. However, this depletion region is largely dominated by the external bias applied, which is relatively temperature independent. Therefore, the depletion region's width should not strongly impact the temperature dependence of the transient response.

While these results are for an increase in ambient temperature, it is worth exploring whether self-heating has an effect on the overall transient behavior. Self-heating is

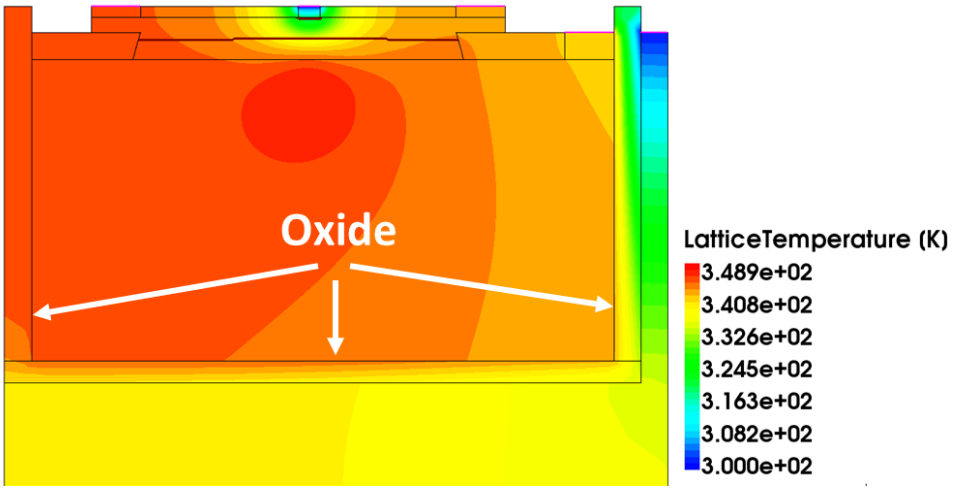


Figure 7.14: TCAD device cross-section indicating lattice temperature at a bias condition of V_{BE} = 0.8 V and V_{CB} = 25 V with self-heating enabled. Dimensions are not drawn to scale.

extremely important in low-voltage and high-speed SiGe HBTs, because with technology scaling, large current densities are required. It is even more relevant in platforms where a buried oxide is present, since the buried oxide impedes the heat flow downwards to the substrate, thus making it harder to dissipate heat.

To better understand the effects of self-heating on the device transients, a thermally calibrated 2-D TCAD model was used. Fig. 7.14 shows the TCAD cross-section of a simple device simulation, and the resulting lattice temperature at a bias condition of V_{BE} = 0.8 V and a V_{CB} = 25 V at an ambient temperature of 24°C. Self-heating was enabled for the simulations by adding thermal surface resistance at the contacts, and the values for the thermal surface resistances were set based on device calibration. Fig. 7.14 clearly indicates that the internal junction temperature can rise well above the ambient temperature ($\Delta T \approx 50°C$).

With self-heating enabled, heavy-ion strike simulations were performed in TCAD. Simulations were performed with a fixed J_E of 1 mA/μm^2 and the V_{CB} was swept from 0–25 V. This particular J_E is an aggressive bias condition, and was used primarily as a worst-case condition. The results are illustrated in Fig. 7.15. The transient peak current as a function of V_{CB} is shown for both simulations with and without self-heating.

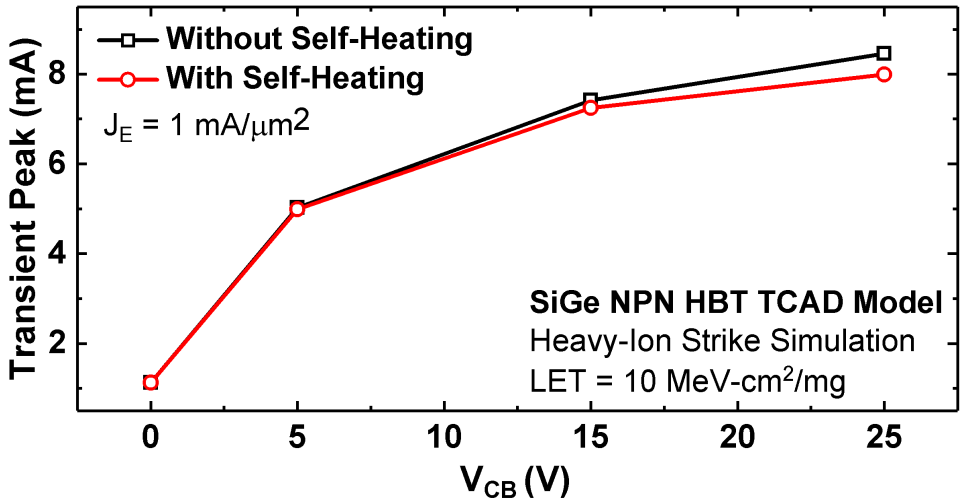


Figure 7.15: TCAD simulation of NPN HBT collector transient peak amplitudes with and without self-heating as a function of V_{CB}.

At low V_{CB}, there are negligible differences between both; as V_{CB} increases, however, the differences become slightly more significant. At a V_{CB} of 25 V, there is less than 10% difference in the peak amplitudes with and without self-heating. Overall, this result is consistent with the temperature behavior observed previously. A higher V_{CB} is required to generate large self-heating, but a higher V_{CB} also makes the transient peak amplitude fairly temperature independent. From a modeling perspective and from a technology scaling perspective, this indicates that modeling and simulating self-heating behavior is not overly significant for heavy-ion strike simulations up to 100°C. Considering only a 10% reduction is observed for a SiGe-on-SOI device, it is unlikely that a bulk platform, even if it is scaled further than this, will be heavily affected by self-heating.

7.4 Summary

This work presents the SET response of a high-voltage (> 30 V) complementary SiGe-on-SOI HBT, and the temperature dependence of this transient response from 30°C–100°C. Due to the unique nature of this SiGe HBT platform, NPN devices show smaller collected charge and transient peak amplitude (2–3X less) than the

PNP devices, contrary to what previously has been reported in the literature. This is found likely to be due to the larger volume of the PNP device, and a larger peak germanium content compared to the NPN device.

Additionally, the temperature dependence of the SET response has been investigated for V_{CB} from 0 V to 40 V. There are two distinct cases: $V_{CB} = 0$ V and $V_{CB} > 0$ V. At a V_{CB} of 0 V, the transient peak amplitude shows a negative temperature coefficient for both NPN and PNP devices. A slight increase in collected charge is also observed due to an increase in transient duration. However, at $V_{CB} > 0$ V, there is no clear temperature dependence observed in measurements. TCAD simulations indicate that both the change in peak electric field and carrier mobility saturates with increasing V_{CB} as a function of temperature. For normal circuit operation, where some V_{CB} is present, it can be stated that the SET response of SiGe HBTs is relatively temperature independent up to 100°C. The findings of the present paper indicate that high temperatures do not significantly degrade the SET response of the C-SiGe-on-SOI platform studied. The results shown suggest that this particular SiGe technology can be used for environments where highly-energetic particles and high temperatures are encountered simultaneously.

The effects of self-heating on the SET response was explored using TCAD. An aggressive bias condition was used to maximize self-heating by increasing V_{CB} up to 25 V. Simulations indicated that even at a V_{CB} of 25 V, less than 10% change in transient peak amplitude is observed. The change is modest even for a SiGe-on-SOI platform, therefore it is unlikely that self-heating will play a large role in the transient response for other bulk platforms.

CHAPTER 8

CONCLUSION

8.1 Contributions

This work has investigated the operation of SiGe HBTs in high-temperature and radiation-rich environments. While SiGe HBTs have traditionally been known to work best at cryogenic temperatures, this work has shown that SiGe HBTs can be used at the other end of the temperature spectrum also. In particular, this work has primarily looked at a high-voltage SiGe-on-SOI technology that is vastly different than typical RF-optimized SiGe HBTs. Most importantly, this work provides a framework on how to go from a device-level analysis to a larger circuit/system for extreme environment operation. The following is a summary of all the contributions of this work:

1. First DC (Gummel, current gain, and BV_{CEO}) and AC characterization (f_T and f_{max}) of a SiGe-on-SOI HBT up to 300°C. SiGe-on-SOI HBTs were shown to exhibit adequate performance even at these elevated temperatures.

2. An analysis of the temperature dependence of the reliability degradation mechanisms in SiGe HBTs. Three different device-level reliability degradation mechanisms were identified and their temperature dependence was investigated using a variety of stress testing methods. While the SOA of SiGe HBTs contracts at high-current operation with increasing temperature, high-voltage and high-power regions were shown to expand at higher temperatures.

3. Development of a wide-temperature calibrated compact model to build high-temperature capable analog building blocks. A cascode current mirror, wide-temperature BGR, and a class-AB push-pull circuit were realized. A design of a BGR with the lowest TC from 24°C-300°C for a silicon-based technology was also shown to be possible with a SiGe technology.

4. A design and demonstration of a high-temperature, high-current gate driver operating at up to 300°C. Up to 2.7 A of current were measured for this driver at high temperature, which is a first for a silicon technology.

5. An analysis of TID effects on a high-voltage SiGe-on-SOI technology. Lower collecting doping was shown to negatively impact the device performance due to TID at high injection. Through TCAD simulations, this was shown to be the effect of STI traps generated through TID.

6. An investigation of the temperature dependence of the SET response in a SiGe-on-SOI technology. The temperature dependence was shown to be heavily dependent on V_{CB}. A V_{CB} of 0 V condition exhibited a negative temperature coefficient while a V_{CB} >0 exhibited very weak temperature dependence. Overall, room temperature was shown to be the worst-case condition for SETs, and higher temperatures do not show any degradation from an SET perspective.

8.2 Future Work

Some of the logical extensions from this work are:

1. Investigate how linearity scales with increasing temperature. This could be particularly important in the context of power amplifiers, which may need to operate at elevated temperatures due to large self-heating.

2. Look at the how the SOA shifts with increasing temperatures under an AC stress condition. While DC stress conditions were investigated in this work, it would

be beneficial from a circuit-level perspective to understand how a dynamic AC signal will impact the stress response.

3. Investigate the effects of device size on the over-temperature SOA. In particular, devices with different perimeter to area ratio.

4. Build upon the gate driver design in this work to make a complete driver that can drive both a high-side and low-side switch along with all the necessary sub-systems [92].

5. Investigate the temperature dependence of TID as a function of V_{CB}.

6. Analyze the differences in the temperature dependence of SETs between SOI and bulk devices. Since the collector-substrate junction plays a large role in the diffusion tail of SETs, it will likely play a large role in the SET temperature dependence.

7. A more thorough investigation into the differences in the NPN and PNP transients in different SiGe-on-SOI technologies.

8. Analyze the temperature dependence of SETs under broad-beam heavy ions. Laser was used in this work, which may potentially impact the temperature dependence of the SETs due to the unknown temperature dependence of the TPA absorption coefficient. A heavy-ion study will help to decouple this dependence.

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